Problem 1: For this problem, consider the adder circuit pictured in fig. 7.5 of the text on p. 389. Assume you are using the CMOS technology documented at the end of the text. Further assume that the load on the S output signal is equivalent to a minimum length n-channel transistor with a width of 100 microns, and your input capacitance must be kept small by making the equivalent W/L ratio for the pulldown switch in the first stage one. Assuming that internal and wiring capacitance is insignificant, pick transistor widths and lengths to minimize delay through the entire circuit. You may match rising and falling delays, and there is no need to use techniques such as tapering within switches since internal capacitance is assumed to be insignificant.

Problem 2: Again using the CMOS technology documented at the end of the text, design a chain of inverters to drive a 10pF load capacitor as quickly as possible (circuit schematic level only). Assume that the polarity of the output is not important so the number of stages can be odd or even. Assume that your first stage has an n-channel transistor with W/L of one, and rising and falling delays are matched throughout. Estimate the energy dissipation of your circuit. If energy was a problem and you had some delay margin, roughly how might you modify your design? Explain.

Problem 3: You can view a long chain of pass transistors as an RC transmission line, similar to a long resistive wire. For the CMOS technology documented at the end of the text, if you had a long pass transistor chain to which repeaters could be added, estimate the optimum spacing of those repeaters to minimize delay. Assume that the transistors are of minimum size (assume minimum width is the same as minimum length), have drain/source regions of reasonable size, and are connected with metal jumpers of 20 microns in length. Explain assumptions. If the logic function of the entire stage would not allow repeaters to be added, what is an alternative approach that could offer similar delay improvements?
Due: Mon., Dec. 10 (or later that week by arrangement)

Option 1: Using the default CMOS technology set up in our CAD tools, design a 16-bit adder. Include a schematic, layout, and short description. Estimate all aspects of performance, at least partially using SPICE simulations. Verify your layout. Try to minimize delay, while keeping other aspects of performance within reasonable ranges. Assume all outputs are driving loads that are equivalent to four basic inverters. If you wish to use dynamic logic, you may assume whatever clock signals you need are available, but clearly explain timing assumptions. A two-person team is expected to go beyond a simple ripple-carry architecture. Further information will be posted on the course web site, including how to submit the designs. [Ref.: Text, pp. 383-407]

Option 2: Using a documented CMOS technology, design a static memory cell as pictured on p. 578 of the text, along with a sense amplifier connected to the bit lines that can read data quickly from one of the memory cells. Assume that there are 256 identical cells connected to the bit lines, and the sense amplifier must drive a load equivalent to four basic inverters. You may assume whatever clock signals you need are available, but clearly explain timing assumptions. Try mainly to minimize delay, but keep other aspects of performance within reasonable ranges. Circuit schematics and layouts can be drawn by hand, but performance should be estimated with SPICE simulations. You do not need to make the sense-amp pitch match that of the memory cell. A short report should document the design and its analysis. A two-person team is expected to add write circuitry and analyze the write operation as well. Check the course web site for further information. [Ref: Text, pp. 457-461, 578-583, 587-589, 596-603]

Option 3: Propose a project of similar complexity to that of either of the first two options. Subject to approval.

Checkpoints:

Mon., Nov. 26: Submit teams & rough, tentative outline of project along with Problem Set 10.

Mon., Dec. 3: Email one paragraph progress report to caz@columbia.edu