Problem 1: Redo problem 6 from problem set 7, this time assuming that the input signal for the inverter comes from the output of a pass logic gate that consists only of an n-channel transistor. How much does the ratio of $W/L$ have to change to maintain the same $V_{OL}$? Assume that the inputs to the pass gate are $V_{OH} = V_{DD} = 3.3v$. Do not ignore the body effect.

Problem 2: Estimate the power dissipation of a precharged logic gate driving a 1pF load capacitor at a clock frequency of 1GHz. Assume the power supply voltage $V_{DD} = 3.3v$. Explain your reasoning, including any approximation you may be making about the statistics of the logic function output value.

Problem 3: Explain roughly some of the reasons that the power dissipation of a digital watch can be so much less than that of a 2GHz Pentium IV microprocessor. Assume they are both built using primarily standard complementary-load CMOS logic gates. Although the CMOS technologies used for these two very different applications could be different in practice, for the purposes of this problem assume they are the same (e.g. threshold voltages, etc.).

Problem 4: If the widths of both the transistors in an inverter are multiplied by 3, and the widths of all the transistors that the inverter is driving are doubled, what happens to the rising and falling delays? Explain. Consider first the case where wiring capacitance is insignificant compared to transistor loading, and then discuss how a significant wiring capacitance would affect your answer (direction & reason only).