Problem 1: Using a sketch, show what gives rise to drain-induced barrier lowering. Also, explain why n-channel transistors in CMOS circuits often have a large drain voltage when a low threshold voltage could cause the biggest problem.

Problem 2: If the power supply wire running to a cell that dissipates 0.1 watt of power with a 3.3v supply is only 40 microns wide and 2 mm long, roughly how much of a 3.3v power supply voltage would actually get to the cell? Explain any approximations. Assume the sheet resistance of the wire is 0.05 ohms per square. What is the current density per unit width in the wire?

Problem 3: If 2 metal wires run next to each other for a distance of 1 mm, they are 0.25 microns apart, and 0.25 microns tall, roughly estimate the capacitance between them. You can ignore fringing in your calculations, but beware that this would add a significant amount of additional capacitance. Also assume that the insulator between them is simply the same oxide you would find under metal and polysilicon wires.

Problem 4: Using the parameters on the inside back cover of the textbook, estimate all the wire resistances & capacitances in the circuit of Colorplate 6 (shortly after p. 14). Assume that contact cuts have a resistance of 1.5 ohms and the diffusions (both n & p) have a sidewall capacitance of 0.1 fF/micron. Draw a complete circuit schematic which includes reasonable models for the wires, including even fairly small resistances – note there is not a unique answer. Only compute the capacitance that is outside the basic transistor models. Explain your main assumptions & approximations.

Problem 5: For this problem you will use SPICE to estimate the equivalent resistance and capacitance of the n-channel transistors (use W/L = 4, L minimum size) in an example 0.25 micron CMOS technology. Documentation on the transistor models and how to run HSPICE can be found on the course web site. Pick reasonable voltages for the following experiments assuming that the typical power supply voltage for the given 0.25 micron technology is 2.5v. For the last two parts, you can wait and hand in the SPICE results along with problem set 6 if necessary. In any case, though, at least hand in an outline of your planned approach with this problem set.

a) If a linear capacitor is discharged through a linear resistor, what percent of the initial voltage is reached within a time given by the product of R and C?

b) First estimate the equivalent total capacitance at the gate by simulating the discharging of the gate through a linear resistor and measuring the time it takes to get to the level computed in part (a).

c) Next estimate the equivalent resistance of the transistor by simulating its use to discharge a linear capacitor and measuring the time it takes to get to the level computed in part (a).