A 5.3 GHz Programmable Divider for HiPerLAN in 0.25μm CMOS

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Programmable divider for a HiPerLAN carrier synthesizer (5 channels)

- Programmability: $D = \{220, \ldots, 224\}$
- Low $V_{dd}$ ($\sim 1.8V$)
- High input frequency (5.15 - 5.3 GHz)
- $\sim 300 \text{ mV}_{pk}$ ($\sim 0 \text{ dBm}$)

Diagram:
- $f_{\text{ref}}$
- $23.5294 \text{ MHz}$
- Phase detector
- Loop filter
- VCO
- $D \cdot f_{\text{ref}}$
Outline

- Divider architecture:
  - Phase switching.
  - Timing issues.
  - Solution: Signal retiming.
- Circuit implementation:
  - High speed ÷2(D-Flip Flop) stage.
- Measurement results.
- Comparison & conclusions.
Phase switching divider

- K phase switches per output cycle: \( \div (4N + K) \)
- No high speed feedback loops around multiple flip-flops.

[Craninckx, JSSC '96]
Glitches

- clock-X to clock-Y when both X & Y are in the same state.

Retiming

- Retimer circuit: enforces control timing for each of the four possible clock transitions.
Phase switching divider with retiming

- Retimer inserted after the second stage.
Retimer: Implementation

- New control generated when both clocks are high.
- Clock and control go through identical paths.
- Feedforward operation $\Rightarrow$ high speed.
High speed ÷2 stages / latches

- Goals: Low $V_{dd}(1.8 \text{ V})$ & high speed(5.5 GHz)
- pMOS: much smaller drive than nMOS.
Pseudo-nMOS low voltage latch

- 0.25µm CMOS, $V_{dd} = 1.8$ V: 3 stage ring osc.
  - CMOS: 2.8 GHz.
  - pseudo-nMOS: 6 GHz.
5.5 GHz ÷2 stage

- 5.5 GHz ÷2 with 300mV\_pk (SE) inputs at V\_dd = 1.8V.
- Disabled by pulling CLK, CLKB inputs to the rails.
Programmable divider

- \{220, ..., 224\} = 216 + \{4, ..., 8\} = 2^3 \cdot 3^3 + \{4, ..., 8\}
- \div 3 \text{ stages-similar to } \div 2, \text{ with gated input branches.}
- 3 stage

LOGIC

- AND gate: combined with the DFF input branches.
Chip Photograph

- divider
- \( \sim 0.09 \text{ mm}^2 \)
- \( 1^{\text{st}} \div 2 \)
- \( 2^{\text{nd}} \div 2 \)
- retimer
- last 4 stages
- o/p buffer
- other logic
- inp
- out
- gnd
Measurements: Sensitivity

- 5.5 GHz operation with $V_{dd} = 2.2$ V, $300mV_{pk}(SE)$ input.
- Changed technology: major discrepancy between models and process.
Phase noise measurement setup

- Dividers contribute phase noise inside the loop bandwidth.
- The inputs to the phase detector are 90° apart.
- Measured noise = 3 dB + noise of each divider.
- Input referred phase noise (@ 5.5 GHz): +47 dB (220x).
Measurements: Phase Noise

- o/p phase noise from 2 dividers & o/p buffers.
- ~ -131 dBc/Hz @ 1 kHz offset.
- 1/f behavior down to 1Hz.
## Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.25 μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Area</td>
<td>0.09 mm²</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>2.2 V</td>
</tr>
<tr>
<td>$I(V_{dd})$</td>
<td>26.8 mA</td>
</tr>
<tr>
<td>$f_{in, \ max}$</td>
<td>5.5 GHz</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>300 mV pk., SE</td>
</tr>
<tr>
<td>o/p phase noise</td>
<td>-131 dBc / Hz</td>
</tr>
<tr>
<td>(5.5 GHz signal i/p)</td>
<td>@ 1 kHz</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>1.8 V</td>
</tr>
<tr>
<td>$I(V_{dd})$</td>
<td>17.4 mA</td>
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<tr>
<td>$f_{in, \ max}$</td>
<td>4.5 GHz</td>
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<tr>
<td>Sensitivity</td>
<td>300 mV pk., SE</td>
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<tr>
<td>o/p phase noise</td>
<td>-133 dBc / Hz</td>
</tr>
<tr>
<td>(4.5 GHz signal i/p)</td>
<td>@ 1 kHz</td>
</tr>
</tbody>
</table>
## Comparison of CMOS dividers

<table>
<thead>
<tr>
<th></th>
<th>Tech.</th>
<th>$f_{\text{in, max}}$ GHz</th>
<th>$V_{\text{dd}}$ V</th>
<th>$P_{\text{d}}$ mW</th>
<th>Input $V_{\text{pk}}$</th>
<th>Phase Noise (input ref.) dBc/Hz$\times1kHz$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>This work</strong></td>
<td>$\div220$ ... $\div224$</td>
<td>0.25 µm</td>
<td>5.5</td>
<td>2.2</td>
<td>59</td>
<td>0.3</td>
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<tr>
<td>De Muer ‘98</td>
<td>$\div8/9$</td>
<td>0.7 µm</td>
<td>1.5</td>
<td>5.0</td>
<td>55</td>
<td>0.16</td>
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<tr>
<td>Kurizu ‘97</td>
<td>$\div4$</td>
<td>0.15 µm</td>
<td>11.8</td>
<td>2.0</td>
<td>20</td>
<td>1.0</td>
</tr>
<tr>
<td>Craninckx ‘95</td>
<td>$\div2$</td>
<td>0.7 µm</td>
<td>1.7</td>
<td>3.0</td>
<td>7.5</td>
<td>1.3</td>
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<tr>
<td>Razavi ‘95</td>
<td>$\div2$</td>
<td>0.1 µm</td>
<td>13.4</td>
<td>2.6</td>
<td>26</td>
<td>1.3</td>
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<tr>
<td>Foroudi ‘95</td>
<td>$\div16$</td>
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<td>1.5</td>
<td>5.0</td>
<td>13</td>
<td>0.35</td>
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<tr>
<td>Cong ‘88</td>
<td>$\div4/5$</td>
<td>0.4 µm</td>
<td>4.2</td>
<td>3.5</td>
<td>0.5</td>
<td>-87.9</td>
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<td>Maeda ‘97</td>
<td>$\div256$</td>
<td>0.2 µm</td>
<td>14.5</td>
<td>0.6</td>
<td>22</td>
<td>1.0</td>
</tr>
</tbody>
</table>
Conclusions

- Programmable divider for HiPerLAN in CMOS.
- Retiming circuit for reliable phase switching.
- 5.5 GHz low voltage ÷2 stage in 0.25μm CMOS.
- Low phase noise achieved at a high input frequency.
Acknowledgments

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