Motivation

- Gain experience in completing the sequence of steps in IC design.
- Measurement of a completed chip- seeing the results in the lab- far more satisfying than design itself.
Course objectives

• Complete design of a chip
  – Design
  – Simulation
  – Layout
  – Verification
  – Package configuration

• Preparation for measurement
  – Design of test setup
  – PCB layout
Measurement of the chip

• 10-12 weeks to process the chip. Will get the packaged chips in June-July.
• Need to go to CISL and measure it on the PCB that is already designed.
Design for fabrication

- Lot more than mere “paper design”. An “all or nothing” proposition. Need to finish all the steps before the chip submission deadline.
- Important to choose a design that is challenging, yet small enough that it can be completed in ~12 weeks.
Process technology

• AMI 0.5μm CMOS
  - 0.5μm minimum length MOS devices
  - 3 metal, 2 poly layers (poly- poly capacitors)
  - High resistivity layer for resistors
  - Power supply voltage ? 5V
  - 1.5mm x 1.5mm die; ~1.2mm x 1.2mm excluding pads
• 28 pin / 40 pin ceramic packages.
Why AMI 0.5µm process?

- Available through MOSIS instructional account.
- Frequent fabrication runs.
- Somewhat “old” (current processes- 0.13µm to 0.25µm).
- Sufficient for our needs- circuits of 100s MHz can be fabricated.
- Upto 5V supply: gives extra flexibility.
Chip design: circuit design

- “Paper design”: block diagram, essential building blocks; sanity check;
- Transistor level circuit design
  - Design and simulation of building blocks
- Integration of building blocks
  - Simulation of the entire design
Chip design: layout

• Layout of individual blocks
  – Drafting the layout
  – Design rule check

• Extraction
  – Extraction of netlist from schematics
  – Layout vs. schematic check
  – Parasitic extraction- resimulation with parasitics; especially important at high frequencies
Chip design: packaging

• Choice of package
  – Number of pins
  – Signal frequencies

• Padframe design
  – Pad layout on the chip(along the periphery)
  – ESD protection circuits
Chip design: finishing the chip

- Placing the design in the padframe
- Connections to the pads
- Extraction of the entire chip and simulation including pads and ESD structures
  - Pads, ESD structures: parasitic loading
  - Bond wire inductors: inductive impedance in series with pins
E4332: Course structure

● First half of the course
  - Lectures on IC design steps
  - Detailed lectures on design

● Second half of the course
  - Design reviews
  - Final presentations
  - I'll be here as a design consultant
Design ideas

- Digital clock
  - 7 segment display, binary display etc.
- AM radio
  - Tuned radio frequency
  - Superheterodyne
Digital clock

- Chain of dividers, display decoders and drivers
Digital clock

• Essential components
  – Timebase
  – Chain of dividers
  – Divided output to display (hh:mm) decoders
  – Time setting

• Extra features
  – Alarm
  – Seconds display
  – Days, months, years, ...
Other projects similar to the clock

- **Timer**
  - Multiple timers
  - Continuous repeat
- **Stopwatch**
  - Multiple laps
- **Chess timer**
AM Radio- TRF (E1201 style)

- Detector loads the tuned circuit
- No amplification - Antenna signal needs to be strong enough
- Can only drive high impedance headphones
AM Radio- active TRF

- Buffer isolates the coil from following circuits
  - Tuned circuit can have a high Q
AM Radio- active TRF

• Buffer isolates the coil from following circuits
  – Tuned circuit can have a high Q
• Amplification possible- can receive weaker signals.
• Can drive a speaker.
• Input tuned circuit bandwidth varies across the AM band(530-1610kHz)
AM Radio- Superheterodyne

- Input tuning can be fixed for AM broadcast band
AM Radio- Superheterodyne

- Channel selection is in the IF stage
  - Constant bandwidth
- More gain before detection.
- Need to have coupled input/local oscillator tuning.
- Can drive a speaker.
Other projects

- You can choose to do something else, but decide by next week! Don't be overambitious
- A/D, D/A converters
- Operational amplifiers
- Single ended to differential converter
Design challenges

- Digital clock, AM radio: low frequency circuits, but
  - Need to complete it!
  - Minimize power
  - Minimize supply voltage
  - etc.