In this laboratory, you will complete the VHDL for your PDP/8 design by implementing the execution controls for the IOT instruction and the interface to the 16550 UART. Please use the design we discussed in class as a starting point. The I/O interface to the UART should have the following entity:

LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY uart_interface IS
  PORT(
    acclr : OUT std_ulogic;
    ioskip : OUT std_ulogic;
    orac : OUT std_ulogic;
    uart_address : OUT std_ulogic_vector(0 TO 2);
    uart_cs0 : OUT std_ulogic;
    uart_read : OUT std_ulogic;
    uart_write : OUT std_ulogic;
    int_request : OUT std_ulogic;
    iop1 : IN std_ulogic;
    iop2 : IN std_ulogic;
    iop4 : IN std_ulogic;
    iop_device_address : IN std_ulogic_vector(0 TO 4);
    rxrdy_bar : IN std_ulogic;
    txrdy_bar : IN std_ulogic
  );
END uart_interface;

You will need to complete the ASM charts for the execution cycles of the IOT instructions.

Since we do not have a VHDL behavioral for the UART (it is actually quite difficult to get this right), you will do most of your testing in hardware. Do try executing a “polling” loop for TTY input and output and make sure
“sensible” commands are being send to the UART. You may want to use your testbench to toggle \texttt{rxrdy\_bar} and \texttt{txrdy\_bar}.

Please turn in your VHDL, the ASM charts for your controller, your testbench, and detailed description of your testing including any relevant waveform plots.