Columbia University  
Department of Electrical Engineering  
EE E6930. Problem Set #5.  
Silicon-on-insulator technology  
Due: April 17, 2002

In the HSPICE simulations you will be doing for this problem set, please use the soiexample technology library which can be found at 
/usr/tech/soiexample/cdslib/soiexample.
The minimum channel length for this technology is $L_{\text{drawn}} = 0.25 \mu m$ and the nominal supply voltage is 2.5 V. The nmos and pmos devices lack explicit body contacts (the body is floating), while the nmos4 and pmos4 devices have explicit body contacts.

1. **History-dependent delay variation in SOI.** Consider a $2\mu /1\mu m$ inverter whose input is stimulated by an ideal voltage source switching back and forth between 2.5 V and ground with a slew time of 100 psec on the transition. The period of the input waveform is 2ns with a 50% duty cycle. Load the inverter with 10fF of capacitance. In HSPICE simulation, start the waveform at 0 and simulate for 10\mu sec.

(a) What is the (output) falling delay of the first switch versus the (output) falling delay of the last switch? What is the (output) rising delay of the first switch versus the (output) rising delay of the last switch?

(b) Using the “state diagram” formalism we discussed in class, the nFET is switching between state 1 (gate high, source and drain both low) and state 5 (gate low, source low, and drain high). The pFET is switching between state 2 (gate low, source and drain both high) and state 5 (gate high, source
high, and drain low). Find the body voltages for the nFET and pFET at the
beginning of the transient for each state (four numbers). Find these same
body voltages at the end of the transient. Explain the delay difference in (a)
in light of these body voltage values. (*Note: To get at the body voltage in
simulation, you will have to use the four-terminal devices and may have to
ground the bodies through a large resistance (> 10 MΩ) to satisfy HSPICE.*)

2. *Parasitic bipolar issues in dynamic logic.* Consider the dynamic
AND gate shown below.

(a) Let all the devices in the dynamic pull-down stack be 10μm wide. All
devices are minimum length (0.25μm). Note that a precharge device has
been included on the internal node \( int1 \) (a common practice in bulk design
to mitigate charge-sharing noise). Assume that \( b \) has not evaluated high for
many cycles do that \( int1 \) has been consistently high for a long time. After this
long period of inactivity, assume that \( b \) now evaluates to high. If \( a7 \) remain zero, simulate what happens at nodes \( dyn \) and \( out \). What is the
source of the charge loss you observe on node \( dyn \)?

(b) Give 2-3 possible circuit “fixes” you could do to alleviate the problem
observed in (a). Simulate at least one of your fixes to verify its efficacy.

3. *Sense-amplifier history-dependent offset and smart-body con-
tacts.* Consider the following SRAM sense amplifier circuit. Consider the
case in which the sense amp has performed many reads of zero on \( bl \) and one
on \( bl_{\text{bar}} \). Assume that the sense-amp clock (\( sa_{\text{clock}} \)) is cycling with a 2
nsec period and 50% duty cycle. You may assume that when the sense-amps
are disabled, \( bl \) and \( bl_{\text{bar}} \) are both precharged to 2.5 V.

(a) Assume that after many reads of zero on \( bl \) and one on \( bl_{\text{bar}} \), a one is
read on bl (zero on bl_bar). Simulate the resulting offset that you would find for the sense amp. Please explain qualitatively the source of this offset.

(b) Consider one of the techniques we discussed in class to mitigate offset by means of a smart body contact and evaluate its efficacy in simulation.