Before beginning this project, you need to complete the tutorial on layout, layout verification, and extraction.

This design is a little more “analogish” that most of the other projects will probably be, but there are no major apologies here because high-performance digital design is analog design in many respects.

In this mini-design project, you will design and lay out the StrongARM latch we discussed in class. The circuit schematic for this gate-isolated, sense-amplifier-based latch is shown below:
Drive the clock input full-rail with an FO1 slew (which would be less than 100 psec). While this latch can be operated with full-rail data inputs (as was done in the case of the StrongARM design as we discussed in class), we will choose to operate this latch with low-swing differential inputs, as might be the case when this latch is used as the receiver of a low-swing serial link. Assume a 300 mV differential input signal around a 1.5-V common-mode voltage. You may assume that this data is slewing at a 10-psec rate. (In you like, you can verify that your latch also works nicely with good old-fashioned full-rail data inputs as well.)

First, play around with device sizes to try to minimize \( t_{\text{clk-q}} \). Assume 10 fF of loading at the output. Start with small devices (which is usually the case with latches, generally) and only size up when you discern a real benefit. Recognize that this delay consists of several components: the time required to build up enough of a differential on \( S_1 \) and \( S_2 \) to begin regenerative action, the time required for regeneration to kick in and pull \( V_1 \) and \( V_2 \) full-rail, and the time required to switch the SR latch. Pay careful attention to the "kludge" device \( M_1 \), since there will be a trade-off in sizing this device between \( t_{\text{clk-q}} \) and aperture time.

Estimate the aperture time by trying to find the narrowest data eye (positioning appropriately against the clock edge) that can be captured by the latch. The aperture time of this latch can be make extraordinarily fast so this may prove difficult to determine with the 10-psec slew rates we are using on the data inputs.

Please lay out your latch circuit, run DRC and LVS, and extract your layout. Because repeat your simulation results from extracted layout and note any differences. Your layout must carefully match the capacitance on nodes \( V_1 \) and \( V_2 \) (also, \( S_1 \) and \( S_2 \)); any mismatch here will translate into a voltage offset at the input. Overall your layout should be made as symmetrical as possible. Your extraction will verify your efforts in matching the wire capacitance of these nodes. (The layout tutorial describes how to backannotate capacitances to the schematic from the extracted layout.) Of course, an additional component of the offset that is not included in these simulation is due to mismatches in the devices (the input devices as well as the devices in the positive-feedback structure). Note that these offset issues are only a concern when you are running the data inputs at low swing. With full-rail swing, these issues do not have to be considered.