References

- CBF, Chapter 8
- DP, Section 4.3.3.1-4.3.3.4
- Bernstein, “High-speed CMOS design styles,” Chapter 3
Basic dynamic gate

- Advantages:
  - Lower capacitive loading because not “redundant” pFET loading (pFET are 2X because of reduced transconductance)
  - Less parasitic diffusion and overlap capacitance on the output node
  - No “fight” to switch. No crowbar currents (ideally). All the current goes to switching the cap.
  - Can switch at lower voltage swings (Vt instead of Vdd/2)
  - Really good for wide OR structures
Cascading domino stages
Problems with dynamic logic

- Monotonic logic (complements require dual rail)
- Correlated precharge and high loading on the clock node (more dI/dt noise and more clock power)
- Evaluate devices in stack slow things down by 20% (would be nice to get rid of it!)
- Reduce noise immunity. Noise in dynamic circuits is more likely to result in functional failure while for static circuits it’s mostly noise-on-delay. Dynamic circuits are actively trading off noise margin for performance!
Noise issues in dynamic logic

- Charge redistribution noise (charge-sharing noise)
- Substrate and n-well noise
- Leakage noise
- Power supply noise
- Coupling noise
Generally…

• Don’t let the gate be really dynamic!
• Put a half-latch around the inverter sized to 1/10 the pull-down strength, although this may have to be adjusted depending on leakage concerns in deeply scaled technology.
• For “small” dynamic gates, you can make the keeper by using non-minimum length transistors. Here’s another trick:
Control of charge-sharing noise

- Eliminating contact helps to reduce internal node cap
- Internal AND nodes can be conditioned to Vdd or Vdd-Vt. Note that this degrades performance!
  - p-channel precharge or
  - n-channel source follower with gate connected to Vdd for Vdd-Vt conditioning (sized 1/10 the strength of the pull-down tree below). This will burn static power and will prevent the dynamic node from being pulled all the way to ground.
- Charge-sharing noise must be checked with worst-case charge storage pattern followed by worst-case evaluation pattern.
- Note that there is a history dependence in dynamic logic
History dependence

- When an n-channel tree evaluates, some nodes not directly connected to ground may also be pulled down (OR structure). These “sneak paths” will slow down the evaluation (we also saw this with static logic, only worse).
- You can sometimes play tricks to eliminate sneak paths by using logically orthogonal signals.
- Devices that are used to mitigate charge sharing by precharging or babysitting internal nodes make this sneak paths even a bigger hit in speed and power.
Substrate and n-well noise

- Switch point determined by $V_t$ in these circuits.
- Substrate (below ground) and nwell (above $V_{dd}$) are generated because substrate/nwell are capacitively coupled to device nodes.
- Plugs! Substrate should be connected to ground as much as possible and nwell should be connected to $V_{dd}$ as much as possible. The DRC rules will check to see that this meets a minimum for latch-up rule. This does not mean that good design practice operates at this minimum.
Leakage noise

• Leakage causes “sag” for wide OR structures, which is precisely where domino gives you the biggest “bang for the buck”

• Leakage currents for TSMC 0.25um are about
Power-supply noise

• With the addition of decoupling capacitance, on-chip resonances are driven to lower frequencies. It is common for significant resonances to exist at around 1/10 the clock frequency.

• One must make sure that the “keepers” are strong enough that the dynamic node can track this power supply noise; otherwise this noise can cause the gate to fail.
Sizing dynamic circuits

- The main idea of domino gates is to skew the circuits and put all the logical evaluation on one edge. This allows you to reduce the logical effort of gates (over their CMOS counterparts). In clocked domino, this is at the expense of additional clock loading. If the “reset” is made asynchronous, this clock loading can be reduced and the demands on the power grid less “synchronous”

- The output inverter is tuned to a strength ratio of 4/1 (pFET/nFET). This speeds the pull-up at the expense of the pull down (and degrades the high noise margin on the input of the inverter).

- Precharge device must be strong enough to comfortable complete the precharge within the clock cycle and meet minimum slew targets.
Sizing dynamic circuits

- Logical effort
Delayed-reset domino

- Getting rid of the evaluate device and delay the precharge clock to avoid a short-circuit current.
- Generally, one needs a “footed” domino every third stage with this technique. The precharge here also dominos.
- There is the extra complexity of generating the delayed clocks.

Better logical effort without the foot!
Domino variations

(a) \[ \text{OUT} = AB (CD + E) \]

(b) \[
\begin{align*}
    f_1 &= (B+C)(D+E) \\
    f_2 &= (B+C)(D+E) \\
    f_3 &= D+E
\end{align*}
\]

(c) \[ FCT \quad A+B \]

(d) \[ \overline{AB} \]

(e) \[ \overline{A}B \]
Does domino logic burn more power?

- Dynamic logic has lower input capacitance
- Dynamic logic adds more capacitance to the clock node (this can be eliminated with self-resetting techniques)
- Any voltage degradation can result in short-circuit currents (keepers help here)
- Some noise mitigation approaches burn power (static source-follower babysit devices).
- Crowbar currents can flow in dynamic during clock transitions (for CMOS, it’s for every transition).
- More transitions in dynamic logic because of the “return-to-zero” characteristics of the logic waveforms.
- Static logic has glitches, which dynamic logic does not have.