EE E6930
Advanced Digital Integrated Circuits
Spring, 2002
Lecture 5. Non-clocked logic: differential and pass transistor logic
References

• CBF, Sections 7.1-7.2
• On-line course reader papers in the “Pass transistor, differential, and current-mode logic” section
NMOS logic
Asymmetric rise/fall
Power and delay
NMOS versus CMOS
DCVS logic
DCVS Pulldown Network
Complementary pass-transistor logic
Complementary pass-transistor logic
Complementary pass-transistor logic
LEAP/LEAN
Double pass-transistor logic (DPL)
Dual Value Logic (DVL)
Differential split level (DSL)
Current-mode logic

\[ EDP = \frac{C^2 V_{DD} \Delta V^2}{I_{bias}} \]