EE E6930
Advanced Digital Integrated Circuits
Spring, 2002
Lecture 12. SOI Devices and Circuits

Columbia Integrated Systems Laboratory
References

• CBF, Chapter 5
• On-line course reader on “SOI”

Many slides borrowed from C. T. Chuang’s 2001 tutorial at VLSI Symposium
Why PD-SOI?

Advantages

- Reduced source/drain parasitic capacitances
- Reduced reverse-body effect in stacked structures
Main Challenges

- Parasitic bipolar effect can result in noise failures

![Diagram showing parasitic bipolar effect and labels for NPN and PNP transistors. The diagram indicates that the collector is N, base is P, and emitter is N. The diagram also shows the drain, source, and body connections. There is an arrow indicating that the collector should be off but conducts current.](image)
Main Challenges

• Parasitic bipolar effect can result in noise failures
• Floating body causes uncertainties in threshold voltage
  – timing
  – noise margin
Body voltage determined by...

- Capacitive coupling of gate, source, drain, and body
Body voltage determined by...

- Diode currents at source-body and drain-body junctions

forward biased

Time scale: < cycle time
Body voltage determined by...

- Diode currents at source- body and drain body junctions

reverse biased

Time scale: >> cycle time
Body voltage determined by...

- Impact ionization currents

hole collection charges body

Time scale: $\gg$ cycle time
Kink effect

- "First" and "second" kink
State diagram view of switching

G = H
S/D = L/L

G = L
S/D = L/H
5a

NFET Body Voltage

0.437 V

0 V

diode leakage

capacitive coupling
State diagram view of switching

NFET

- G=H, S/D=L/L
- G=L, S/D=L/H
- G=L, S/D=L/H
- G=L, S/D=H/L
- G=H, S/D=L/H
- G=H, S/D=H/L
Hysteretic $V_T$ Variation

- Long Time Constants for Body Charging & Discharging
  - Impact Ionization Current
  - Junction Leakage/Current
  - GIDL
- Body Potential during Switching Transient Determined Primarily by
  - External Biasing
  - Capacitive Coupling
- Charge Imbalance through Switching Cycle
- Circuit Behavior Depends on Prior States and Switching Patterns
Static CMOS Inverter: Initial Input at “Low”

- nFET $V_B$ Determined by Back-to-Back Diodes
- pFET $V_B$ at $V_{DD}$ Initially
- pFET $V_B$ before Input Falling Transition Determined by Capacitive Coupling
Static CMOS Inverter: Initial State

- Initial Input at “Low”
  - $n$FET $V_B$ Determined by Back-to-Back Diodes
  - $p$FET $V_B$ at $V_{DD}$ Initially
    - $p$FET $V_B$ before Input Falling Transition
      Determined by Capacitive Coupling
- Initial Input at “High”
  - $n$FET $V_B$ at GND Initially
  - $n$FET $V_B$ before Input Rising Transition
    Determined by Capacitive Coupling
  - $p$FET $V_B$ Determined by Back-to-Back Diodes
- Delay Disparity at Beginning of Switching Activity
Hysteresis in Static CMOS Inverter: Initial State

- Large Delay Disparity at Beginning Due to Different Initial States
  - $V_{BS}$ Determined by Balance of Forward Diode Current & Reverse Leakage
  - $V_{BS}$ Determined by Capacitive Coupling
- Steady-State Independent of Initial States
  - Determined Only by $\Delta Q$ through Switching Cycle
  - Reached when $\Delta Q$ through Switching Cycle Equal to Zero
- Steady-State Delay Can Be Outside the Bound of The Two Initial-State Delays

1.8 V, $L_{eff} = 0.145 \ \mu m$, $W_p/W_n = 2$,
1.0 ns Period, 50% Duty Cycle, 100 ps Input Slew
Initial Input at “Low” (L-H) / ”High” (H-L)
Parasitic Bipolar Effect and Reduced $V_T$ Leakage

- Parasitic Bipolar Leakage through “Off” Tx
  - “Off” Tx High in Stack or in Pass-Gate Configuration with Source & Drain Conditioned to “High”, Resulting in High Body Voltage
  - Source Subsequently Pulled Down
    - Parasitic Bipolar Current
    - Reduced-$V_T$ FET Leakage
  - Dynamic Node Voltage Droop
- Problem Circuit Topologies
  - Stacked OR-AND Structures
    - Dynamic OR
  - Pass-Transistor Based Circuits
    - High Fan-In Mux
    - Pseudo-2-Phase Dynamic Circuits
  - Multi-Level Voltage-Switch Current Steering Circuits
    - Dynamic CVSL XOR Circuit
Dynamic Carry Look-Ahead Adder in PowerPC 750

- Parasitic Bipolar Current Causes Dynamic Node Voltage Droop
- Noise Propagates to Next Stage
- Cumulative Effect of Parasitic Bipolar Current and Propagated Noise Cause Data Corruption after 3rd Stage in The Chain

(M. Canada et al., ISSCC, 1999)
Dynamic Circuit Techniques for SOI

• SOI Unique Features
  – Reduced Charge Sharing Effect due to Reduced Junction Capacitance
  – Less Delay Dependency on Stack Ordering due to Absence of Reverse-Body Effect

• Dynamic Circuit Techniques
  – Pre-discharging Intermediate Nodes
  – Re-ordering Pulldown Stack
  – Cross-connecting Fingered Stacks
  – Force Parasitic Bipolar Current to Occur during Precharge Phase
  – Re-mapping Boolean Logic
  – Complex Domino
Pre-discharging Intermediate Nodes

- **Bulk Design**
  Intermediate Nodes Precharged to $V_{DD}$ to Minimize Charge Sharing

- **SOI Design**
  Intermediate Nodes Discharged to Prevent Parasitic Bipolar Effect

![Bulk Design](image1.png)

![SOI Design](image2.png)
SOI Dynamic Circuit Techniques

(D. H. Allen et al., ISSCC, 1999)
Summary - Parasitic Bipolar Effect and Reduced $V_T$ Leakage

- Present Only in Certain Circuit Topologies
- Effect Reduced by Technology and Device Design
  - Source/Drain Extension to Reduce Emitter & Collector Area
  - Retrograde Channel Doping to Increase Effective Bipolar Gummel Number
  - Leaky Body-Source Junction to Reduce Bipolar Current Gain
- Supply Scaling
  - Parasitic Bipolar Effect Becomes Less Significant
  - Reduced $V_T$ Leakage Becomes More Serious
- Experimentally, Parasitic Bipolar Effect Does Not Appear to Increase as $L_{eff}$ Is Reduced/Scaled
- $< 10 \, \mu A/\mu m$ in Well-Designed State-of-The-Art Devices
- Design Impact
  - Significant Design/Sizing Effort
  - Sizing Up Keeper Device (Few % in Perf.)
  - Selective Body Contacts (Few % in Area)
  - Alternative Implementations
  - Circuit Techniques to Minimize Effects
SRAM circuit issues

SRAM write
SRAM circuit issues
Body contacts
SRAM circuit issues
DTMOS

- Body is employed as a backpate, lowering the Vt when trying to turn the device on and increasing the Vt when turning it off.
- Adding significant capacitance to the gate and significant Miller capacitance.
- Large RC delay associated with the body contact, so performance advantage not achieved in practice.
- Operating voltages limited to 0.5 V or less to prevent S-B/D-B junctions from becoming forward-biased.
Smart Body Contact for High-Performance Applications

• High Voltage
  – Connect Body to Gate Results in Large Diode Leakage
  – Circuits Stressed at Elevated Voltage and Temperature During Reliability Screening
• Viable Smart Body Contact Scheme
  – Significant Performance Improvement
  – Withstand High Voltage
  – Minimum Area
  – Tolerant to Distributed RC of Body Contact
• Type-1: Improving Noise Immunity and/or Device Matching while Preserving Performance Advantage of Floating Body
• Type-2: Maximizing Performance by Charging Up Body before Device Switches
Smart Body Contact: Dynamic Body Discharge

Discharge Body during “Off” State to Prevent Very High Body Voltage
Reduce “On” Pass-Tx Output Voltage Overshoot
Reduce Initial-Cycle Parasitic Bipolar Current in Pass-Tx
Turn off Body Discharge Path When Tx about to Be “On” to Maintain Performance Advantage of Floating Body

Discharge devices and inverter are small

(J. B. Kuang et al., IEEE Int. SOI Conf., 1999)
Dynamic Body Discharge: Latch-Type Sense Amplifier

Improve Device Matching and Noise Margin
Maintain Performance Advantage of Floating Body

To bit switches

Bitline_T

Bitline_C

sense_amp_rst

sense_amp_set

Discharge nFETs

Discharge nFETs

Data_T

To data out

Data_C

(J. B. Kuang et al., IEEE Int. SOI Conf., 1999)
Dynamic Body Discharge: Sensing Performance

A: Dynamic Body Discharge, 0.7 V Initial Body Bias
B: No Body Discharge, No Initial Body Bias
C: No Body Discharge, 0.7 V Initial Body Bias

(J. B. Kuang et al., IEEE Int. SOI Conf., 1999)
Smart Body Contact
(Body Driven by Subsidiary Tx of The Same Type)

Gate Cap. of Subsidiary Tx
Add to Input Cap.
Body of Primary Switching Tx
Not Charged until Input Rises
above $V_T$ of Subsidiary Tx

Drain Cap. of Subsidiary Tx
Add to Input Cap.
Body of Primary Switching Tx
Charged Immediately Once
Input Switches

(I. Y. Chung et al., IEEE Int. SOI Conf., 1996)
(J. Gil et al., ISLPED, 1998)
Smart Body Contact

0.25 \( \lambda m \) \( L_{\text{eff}} \) and \( V_{\text{DD}} = 1.2 \) V

7-Stage Inverter Chain at 100 MHz

(b) Offers 35% Delay Improvement over Conventional Ckt

(b) Offers 20% Delay Improvement over (a)

(J. Gil et al., ISLPED, 1998)
Charge Flooding: Latch-Type Sense Amplifier

Flexible Timing for Both Edges

(J. B. Kuang et al., IEEE Int. SOI Conf., 2000)
Charge Flooding: Sensing Performance

Body Voltage Mismatch = 600 mV

Original Circuit: Sensing Fails !  Charge Flooding: Restores Tracking

(J. B. Kuang et al., IEEE Int. SOI Conf., 2000)
Charge Flooding: Sensing Performance

Faster Bitline Differential Voltage Development
Faster Sensing Resolution

(J. B. Kuang et al., IEEE Int. SOI Conf., 2000)
CMOS Device Scaling and SOI

- 0.25 µm - 0.15 µm
  - Competition against Rapidly Evolving Bulk CMOS
  - SOI Limited to Special (Rad.-Hardened, High-V) Applications
- 0.12 µm - 0.07 µm
  - Scaling towards End of Road Map for Bulk CMOS
  - Bulk CMOS Evolution Decelerates to Slower Pace
  - SOI Stands Better Chance for Mainstream Applications
    - Fully-Depleted (FD) SOI Device \((t_{Si} < 50 \text{ nm})\)
    - Partially-Depleted (PD) SOI Device \((t_{Si} \approx 150 \text{ nm})\)
- 50 nm - 25 nm
  - Beyond Bulk CMOS Scaling Limit
  - New Device Structures
    - Thin-Body SOI Device \((t_{Si} < 1/4 \text{ } L_G)\)
    - Dual-Gate SOI Device \((t_{Si} < 1/4 \text{ } L_G)\)
Thin-Body SOI Device

- $t_{Si} < 1/4 \ L_G$ to Suppress DIBL and Improve SCE
- Lightly-Doped Body: Improve Mobility and Reduce Tunneling
- Gate Workfunction Engineering (Mid-Gap, Poly-SiGe, etc.)
- High $k$ Gate Dielectric
- Fan-Out Source/Drain to Reduce Series Resistance
Dual-Gate SOI Device

- All the Benefits of Thin-Body SOI Device
- 2 Channels with Twice Gate Capacitance (for FG/BG Tie)
- Max Control of Channel Potential
  - Best SCE ($L_{eff} < 25$ nm)
  - Steeper Subthreshold Slope (60 mV/dec vs 85 mV/dec for bulk)
- Potential for Achieving Ballistic-Limit Current in nMOS*
  * (K. Kim and J. G. Fossum, SRC Techcon, 2000)
  - Lightly-Doped Body, Low Transversal Field
  - 2X to 2.4X Mobility Improvement
- No Performance Loss in Stacked Devices due to Body Effect
- FG/BG Mis-Alignment Costs Extra $C_{OVERLAP}$ & Loss of Current Drive
Quasi-Planar Double-Gate Fin FET

- Process simplicity and compatibility with conventional planar CMOS technology
- Gate straddles thin silicon film
- Current flows parallel to wafer – Quasi-Planar structure
- Quantized device width (Width = n x Fin Height)

(S. H. Tang et al., ISSCC, 2001)
Double-Gate Fin FET: Fin Formation and Layout

- Etching with spacer mask
- Sub- lithography pitch and width
- Fins packed narrower and tighter than gate

Same layout techniques as conventional CMOS
S/D directly strapped with metal
Top & sides of each fin contacted

(S. H. Tang et al., ISSCC, 2001)