References

• On-line course reader on “Low power design”

Some slides adapted from T. Sakurai’s ISSCC2001 tutorial on low power design
### Vdd/Vt tricks

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<th>Active</th>
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Clustered Voltage Scaling for Multiple $V_{DD}$’s

Conventional Design

CVS Structure

Level-Shifting F/F

Critical Path

Critical Path

Lower $V_{DD}$ portion is shown as shaded

Once $V_L$ is applied to a logic gate, $V_L$ is applied to subsequent logic gates until F/F’s to eliminate DC current paths. F/F’s restore $V_H$.

Slave-Latch Level-Conversion F/F
If you don’t need to hussle, \( V_{DD} \) should be as low as possible

**Energy consumption is proportional to the square of \( V_{DD} \).**

**\( V_{DD} \) should be lowered to the minimum level which ensures the real-time operation.**
Variable clock and supply generation

Diagram:

1. Desired rate → Lookup table → Desired voltage → Voltage regulator → \( V_{bat} \) → \( V_{DD} \)

2. Reference clock → Rate compare → Programmable lookup table → Voltage regulator → Ring oscillator → Clock → \( V_{DD} \) → Digital system

3. Clock → \( N \) → Phase compare → Voltage regulator → Matched ring oscillator → Digital circuits
DC-DC converters

• Three types
  – Switching regulators (efficiencies that can approach 100% as the components are made more “ideal”; in practice, 75%-90% efficient)
  – Linear regulators
  – Switched capacitor converter
PWM switching DC-DC converter

Unregulated dc

Low-Pass Output Filter

Regulated dc

PWM

Error Amplifier

Frequency $f_s$

Duty Cycle $D$

$V_{ref}$

$V_{in}$

$V_o$

$R_L$

Pass device

Rectifier device

$V_o = V_{in} D$
PWM waveforms

\[ \Delta I = \frac{(V_{in} - V_{out})DT}{L_f} = \frac{V_{in}D(1 - D)}{L_f f_s} \]

\[ \Delta V = \frac{1}{2} \frac{\Delta I}{2} \frac{T}{2} \frac{1}{C_f} = \frac{\Delta I}{8C_f f_s} = \frac{V_{out}(1 - D)}{8L_f C_f f_s^2} \]

High frequency, smaller filter size.
Sources of loss

• Resistances in the switches (transistors), inductors, capacitors.
• Gate drive loss in driving the switches
• Timing errors that prevent the power transistors
Dead-time control for zero-voltage switching
Digital PWM circuits

Fast clocked counter
Digital PWM circuits

Tapped delay line
Linear regulator

Efficiency can never be greater than $\frac{V_o}{V_{in}}$
Switched capacitor supply

\[ E_{\text{diss}} = \frac{1}{2} \frac{C_1 C_2}{C_1 + C_2} \left( V_{1(\text{initial})} - V_{2(\text{initial})} \right)^2 \]

\[ \eta = \frac{V_o Q_L}{V_{in} Q_{in}} = \frac{V_o}{V_{in}} = \frac{V_{in} - \Delta V}{V_{in}} = 1 - \frac{\Delta V}{V_{in}} = 1 - \frac{I_L T}{C_{out} V_{in}} \]