EE E6930
Advanced Digital Integrated Circuits
Spring, 2002
Lecture 1. CMOS Device Technology
Course Logistics

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• Class web page
  http://www.cisl.columbia.edu/courses/spring-2002/ee6930/
Tools/Technology

- This course will make extensive use of the CISL tool set for problem sets and mini-design projects. Tutorials will be provided on-line as needed.
- You must have accounts set up on the CISL machines in Mudd 1218. A sign-up sheet will be passed around in class.
- Remote access is possible using ssh (telnet and rlogin are not possible for security reasons). If you are a remote user, you are responsible for your own “local” tools support.
- We will make use of the TSMC 0.25um mixed-signal process for our design work. Design manuals for this technology will be made available through the class website.
Books

• Textbook
  Dally and Poulton, “Digital Systems Engineering,”
  Cambridge University Press, 1998. (DP)

• Other useful books
References

• DP, Sections 4.1-4.2
• CBF, Sections 2.1-2.2, 3.1-3.3
• Papers (both in on-line course reader)
"Textbook" long-channel MOSFET

\[ V_T = V_{FB} + 2|\phi_F| + \frac{Q_s}{C_{ox}} \]

\[ Q_s = qN_A X_d \]

\[ 2|\phi_F| = \frac{qN_A X_d^2}{2\kappa_s \varepsilon_o} \]

\[ Q_s = \sqrt{2\kappa_s \varepsilon_o qN_A 2|\phi_F|} \]
"Textbook" long channel MOSFET

\[
Q_n = C_{ox}(V_{GS} - V_T)
\]

\[
dV = I_D dR
\]

\[
dV = I_D \frac{dy}{W \mu_n Q_n(y)}
\]

\[
dV = I_D \frac{dy}{W \mu_n C_{ox}(V_{gs} - V_T - V)}
\]

\[
\int_{V_{DS}} dV \left( W \mu_n C_{ox} \right)(V_{gs} - V_T - V) = \int_{0}^{L} I_D dy
\]

\[
I_D = \frac{W \mu_n C_{ox}}{L} \left( (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)
\]

\[
I_D = \frac{W \mu_n C_{ox}}{2L} (V_{gs} - V_T)^2
\]

(Vgs – Vt) is referred to as the gate overdrive.
“Real” deep submicron MOSFET

TSMC 0.25um

Velocity saturation

\[
I_{\text{DSat}} = \frac{W \mu_n C_{\text{ox}} (V_{\text{GS}} - V_T)(V_{\text{GS}} - V_T)}{2L}
\]

\[
I_{\text{DSat}} = \frac{WC_{\text{ox}} (V_{\text{GS}} - V_T) V_{\text{sat}}}{2}
\]

Vt = +/- 0.53 V
Idsat = 600 uA/um for NMOS
Idsat = 270 uA/um for PMOS
Tox = 5.4 nm
**“Classical” scaling**

<table>
<thead>
<tr>
<th></th>
<th>Constant V, long</th>
<th>Constant E</th>
<th>Constant V, short</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device dimensions</td>
<td>(1/k)</td>
<td>(1/k)</td>
<td>(1/k)</td>
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<tr>
<td>Doping concentration</td>
<td>(k)</td>
<td>(k^2)</td>
<td>(k^2)</td>
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<tr>
<td>Voltage</td>
<td>(1/k)</td>
<td>(1)</td>
<td>(1)</td>
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<tr>
<td>Electric field</td>
<td>(1)</td>
<td>(k)</td>
<td>(k)</td>
</tr>
<tr>
<td>Depletion widths</td>
<td>(1/k)</td>
<td>(1/k)</td>
<td>(1/k)</td>
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<tr>
<td>Gate capacitance</td>
<td>(1/k)</td>
<td>(1/k)</td>
<td>(1/k)</td>
</tr>
<tr>
<td>Current</td>
<td>(1/k)</td>
<td>(k)</td>
<td>(1)</td>
</tr>
<tr>
<td>Delay=CV/I</td>
<td>(1/k)</td>
<td>(1/k^2)</td>
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</tr>
<tr>
<td>Power = IV</td>
<td>(1/k^2)</td>
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<td>(1)</td>
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<tr>
<td>Power-delay product</td>
<td>(1/k^3)</td>
<td>(1/k)</td>
<td>(1/k)</td>
</tr>
<tr>
<td>EDP</td>
<td>(1/k^4)</td>
<td>(1/k^3)</td>
<td>(1/k^2)</td>
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</tbody>
</table>
Scaling: The reality

- Threshold voltage cannot be lowered below 0.2 V (maybe another 0.2 V) for tolerances before subthreshold leakage grows too large (a few 10’s of nA)
- Oxide thickness limited to 1.5-2.0 nm before oxide tunnelling current exceeds 1-10 A/cm²!
- DRAMs will have much tighter leakage requirement!
Scaling limits: Subthreshold leakage
Scaling limits: oxide tunneling

T-independent QM tunneling
More complex Vt/Vdd tradeoff
Controlling short channel effects

Dealing with the consequences that built-in voltages do not scale

Classic Vt rolloff
LDD extensions
Retrograde and halo doping
Effect of halo doping on Vt rolloff
Body effect
Capacitances

(a) $V_{GT} < 0$
(b) $V_{GT} > 0, V_{DS}$ small
(c) $V_{GT} > 0, V_{DS}$ large
Process variations

Chip mean across wafers, lots

On-chip ACLV

Occurrences

Channel Length