Columbia University  
Department of Electrical Engineering  
EE E6930. Advanced Digital Integrated Circuits  
Final Topics

The final will cover all the material in the course, although there will be certainly be more emphasis on the material in Lecture 9 and later. The questions will have a style similar to those on the midterm (you now know what to expect!)

- Device physics of advanced CMOS processes
  - Basic long channel MOS IV characteristics
  - Scaling and the limits of scaling
  - Velocity saturation effects
  - Subthreshold conduction and gate leakage issues
  - Controlling short-channel effects with doping (retrograde and halo doping)
  - DIBL
  - Body effect
  - MOS capacitance models
  - Process variations

- Basic static CMOS
  - Basic delay metric for static logic (FO1 and FO4 delay) and their relation to device $f_T$
  - Logical-effort-based sizing of static logic gates
  - “Trajectory” analysis of switching gates and static voltage transfer characteristics
  - Static dc noise margins
  - Performance of stacks; delay estimation of stacks
  - Energy-delay product analysis of static logic
- Effect of slew of delay
- History and pattern dependence of delay in static logic

- Interconnect modelling
  - Interconnect scaling issues
  - Definition of Elmore delay and calculation for RC trees
  - AWE-based analysis of RC networks to render pi-model, pole-residue macromodels.

- Differential, pass-transistor, and current-model logic
  - DCVS logic
  - Pass-transistor logic: delay analysis, noise issues
  - Current-mode logic: energy-delay product analysis

- Clocked storage elements
  - Pass-gate and TSPC-based transparent latches
  - Flip-flop based design: double latch, sense-amplifier flop, clock-chopped flop
  - Latch and flop performance analysis: aperture time (setup and hold times), \( t_{\text{sk-\text{h}}} \)

- Domino logic
  - Timing "checks" necessary to ensure domino logic works correctly
  - Noise issues in domino logic and circuit techniques to control them
  - History and pattern dependence of delay in domino logic
  - Sizing domino logic for performance

- Latch and clock methodology
  - Two-phase design with static and dynamic logic: cycle stealing, race conditions, relaunch penalty
  - Delayed-reset domino: clock reset
- Self-resetting logic: self-timed reset, pulse-mode signalling, pulsed SRCMOS latches

- Self-timed pipelines
  - General concepts of pipelining and wavepipelining
  - Controlling the movement of data with request-acknowledge control.
  - Asynchronous pipelines based on implicit latching properties of dynamic logic (e.g. Williams’ PS0 pipeline)
  - Asynchronous pipelines based on transparent latches.

- Low-power techniques
  - Simple ideas of signal and switching probabilities
  - Performance-power tradeoffs in $V_{DD}/V_T$ space
  - Sleep transistors for controlling leakage
  - Active substrate biasing techniques. Charge-pump circuits.
  - Simple adiabatic logic based on slow clock power source. Resonant circuits and stepwise charging circuits for creating pulse power supply.
  - Multiple-$V_{DD}$ design. Level-conversion circuits.
  - Basic dc-dc converters: Buck converters, linear regulators, switched-capacitor supplies.

- SOI devices and circuits
  - Partially-depleted versus fully-depleted devices
  - Advantages of PD-SOI
  - Challenges of the floating body: parasitic bipolar leakage and history effect.
  - “State diagram” abstraction of SOI body physics
  - Circuit techniques for domino design in SOI
  - Smart body contacts. Applications in sense amplifiers.
• SRAM design
  – Basic 6-T SRAM cell. Basic sizing for writability and read stabili-
    ty.
  – Basic SRAM organization: blocks and divided word-line architec-
    ture.
  – SRAM datapath design: column multiplexing and sense-amplifiers
  – Pulsed word-lines and replica timing for low power.

• DRAM design
  – 1 T DRAM cell. Capacitor technology.
  – Open and folded bit-line architectures.
  – Basic DRAM circuits.
  – Overdriving techniques to improve sense-amp performance.
  – DRAM architectures: FPM, EDO, SDRAM, DDR SDRAM, Rambus-
    DRAM

• Power and clock distribution issues
  – Power distribution. Virtues of grid-based power networks, C4 tech-
    nology.
  – Delta-I noise and decoupling capacitance. Power-supply reso-
    nances.
  – Metrics of global clock distribution: skew, jitter, power, area, slew
    rates
  – Clock trees and clock grids. Tree-driven grids.
  – Inductance in the clock distribution.
  – Active deskewing circuits.

• PLL/DLL design
  – Classical digital PLL: linear, continuous-time model.
- PLL building blocks: phase detector, charge-pump, VCO, divider
- PLL jitter (phase noise) behavior
- Second-order loop filters and feedforward compensation techniques
- Maneatis-style PLL.
- DLL linear, continuous-time model.
- Maneatis-style DLL.
- Digital DLL.
- Problems with DLL’s inability to cycle slip: semidigital dual DLL

• Basics of Verilog-A modelling

• Basic ESD Design
  - Basic ESD models: human-body model, machine model, charged device model
  - Basic ESD clamp devices: diode, nMOS transistor (as lateral NPN), SCR
  - “Improvements” to the nMOS transistor clamp: gate-coupled nMOS, pnp-driven nMOS, substrate-triggered nMOS, substrate-pumped nMOS
  - Mixed-voltage ESD circuits
  - BIFET power-supply clamping.
  - ESD issues for high-frequencies, analog, and RF.

• High-speed I/O interfaces
  - Source-synchronous links
  - Transceiver circuits