dc_shell < tsmc025.cmd > dc.log &

One the job has completed, you will need to import the results into Composer. Choose Run → Import Design. This will run the import utility in background. When it has completed (successfully), there will be a library called DESIGNS in your Library Manager. This contains the Synopsys synthesis results. You will now want to copy over the schematics for counter and controller as well as the symbol and schematics for counter_DW01_incdec_7_0 into tutorial_syn. You should open the new (synthesized) schematics and check and save them, since this is not done automatically on import.

Our default command file also creates a timing (slack) report.
In this tutorial, we will synthesis a design from VHDL into our standard-cell library (digLib_tsc) using Synopsys Design Compiler. You should run synthesis early in the design cycle to get an estimate of the area of
You will find important documentation in the following places:

- Synopsys documentation. PDF (use acroread) can be found at
  /var4/synopsys/doc/online/top.pdf

- Library documentation. PDF can be found at
  /usr/tech/tsmc025/artisan/sc_99q1v1/doc

First copy the library tutorial_syn from /u2/ee4332/cdslib/tutorial_syn to your home directory and add it to your library search path. We will be synthesizing a piece of VHDL which codes the “classic” traffic light controller of Mead and Conway. Open up the schematic window for traffic_light. Bring up the VHDL toolbox from Tools → VHDL Toolbox. Choose Setup → Hierarchy and set things up like you've done in the past for simulation. Then choose Commands → Synthesis. This should automatically netlist and analyze your schematic, bring up the “CSI Initialization” form. Fill in the “Run directory” field if you would like it to be something different from the default dci.run1. Okay this form to establish a run directory for Synopsys. You now get the CSI form (Cadence-Synopsys Interface). Choose Run → Build command file, which create a file for use called netlist.inc in your run directory which contains the appropriate analysis commands for Design Compiler to find your VHDL.

Now copy over the default command file for your synthesis process from
/usr/tech/tsmc025/synopsys/scripts/tsmc025.cmd
to your run directory. Now we will edit this file. Change TOPCELLNAMEHERE to be the name of your top cell view. The clocks are already configured to have a 10-nsec cycle time.

Now to invoke Design Compiler, from your run directory, execute