• Introduction to VHDL (Important for all the hardware designers.)

• Introduction to MPEG-1, Layer-3 (Important for all the software designers.)

• Overview of the ADSP-2181 architecture subset we’ll be implementing and overview of the microarchitecture of our design

• DAC fundamentals and mixed-signal design issues

• Parallel-port protocol and memory interface timing (reading a datasheet!)

• Multiplier design (Important for the people designing the MAC unit.)

• SRAM design issues (Important to the people designing the SRAMs).

• Introduction to synthesis and place-and-route

• Chip integration, floorplanning and global issues (clock, power)

In addition, there will be “self-guided” tools tutorials on logic simulation, synthesis, place-and-route, floorplanning, and timing.

Project schedule (rough)

• Week of 1/31. Preliminary group assignments. I will meet with each group with week to help kick things off, since there are specialized issues each group will have to deal with.

• Weeks of 2/28 and 3/6. Design reviews.

• Week of 5/1. Final project presentations.
• Glasser and Dobberpuhl, *The Design and Analysis of VLSI Circuits*, Addison-Wesley.

• Uyemura, *Circuit Design for CMOS VLSI*, Kluwer.

• Bhasker, *A VHDL Primer*, Prentice-Hall.


**Grading:** All of the grading is based on the project:

• Design review: 25%

• Weekly group status: 25%

• Final project report and presentation: 50%

A portion (but not easily quantifiable) part of your grade will involve how well you have worked together in your team. The "quality" of the curve will be determined by the overall success of the project.

**Lecture schedule**

In the lectures, we will cover various topics of interest in the design. I am expecting that the lectures will only last the first half of the semester. After that, we will have weekly team meetings, either with individual teams or with several teams together. We will also schedule some "mid-semester" design reviews in which each group will present to the entire class. Some of the lectures may be "over-the-head" of some of the students in the class, because of the specialization that each of your will be doing as part of the design. For example, the software people may not understand the SRAM design lectures. Similarly, the SRAM design people may not understand the details of the MP3 algorithm. By the same token, these lectures are not expected to be comprehensive in your "area of specialization." They will only provide an overview. The lecture topics I expect to cover include:
mixed-signal noise concerns. This group will also take the lead in the mixed-signal aspects of the final design verification.

- **MAC design.** This group will be responsible for the VHDL, circuit, and layout of the multiplier-accumulator, the critical element of the DSP datapath. This will be custom digital design.

- **ALU and shifter design.** This group will be responsible for the VHDL, circuit, and layout of the ALU and shifter, the other major elements of the datapath. This group will also be responsible for the execution-unit integration, working together with the MAC-design group.

- **SRAM design.** This group will be responsible for the SRAM design of the split on-chip memory.

- **Instruction-unit design (program control and address generation).** This group will be responsible for the control logic design of the processor, instruction decode, and address generation. Mostly logic design with standard-cell implementation, but some custom circuit design possible.

- **Memory/host interface group.** This group will be responsible for the logic, circuits, and layout associated with the interfaces to the flash memory and to the parallel port. Mostly logic design with standard-cell implementation, but some custom circuit design possible.

Toward the end of the design, I expect a loose reorganization of the teams as we address the global design issues. This includes chip integration, final routing and extraction, and final timing verification. In addition, system simulation, including the interface to the analog and the hardware-software co-simulation will have to be done.

**References:**
The following books, which you might find useful as references, are on reserve in the Engineering Library:


**Goal:** In this course, we will be designing an MP3 decoder chip for a portable player. In the first class, we will come up with a code name for our project, an essential component of any project kick-off. The chip will interface to a PC through a parallel-port interface, to off-chip Flash memory for code and music, to two crystal oscillators, and to stereo headphones. This is an extremely ambitious project involving both hardware and software design and will require the entire class working together as a team to be successful. To make this job tractable, we will be matching the instruction set of the Analog Devices ADSP-2181 programmable 16-bit DSP (although not supporting all of the instructions and features of the ADSP-2181!). This will allow us to do the software development in C, which is essential for an algorithm of this complexity. Furthermore (and perhaps more importantly), it will allow the software development to be done in parallel with the hardware development. In the end, we will perform simulation of the hardware and software together before releasing the chip.

The class will be divided into teams of 2-4 students, each working on different parts of the design. This parallelism is essential to getting the job done, but also makes it all the more important that each of the teams communicate to make sure that all of the pieces will work together. I will be functioning as the project manager and technical lead for the project, trying to keep the whole thing coordinated and on schedule. For most of the semester, I expect the groups to break down roughly as follows (with the associated tasks roughly defined):

- **MP3 software development.** Responsible for debugging and testing a fixed-point implementation of MPEG-1, Layer-3 audio on the PC. Once this works, you will be compiling and debugging this on the ADSP-2181, using the development tools and demo boards from Analog Devices. Code size will be a very important issue (as it is in any embedded application). In the end, this group will be responsible for verifying that the software works correctly with our hardware in simulation.

- **Analog interface.** This group will be responsible for designing the DACs which will go on chip and the interface to the headphones. Data will be fed to the DACs at one of three sample rates: 32 kHz, 44.1 kHz, or 48 kHz, as specified in the MPEG standard. This group will be responsible for the circuit design and layout including proper consideration of
Columbia University
Department of Electrical Engineering
Spring, 2000

Course: EE E4332, VLSI Design Laboratory.

Instructor: Ken Shepard

E-mail: shepard@ee.columbia.edu

Office: 1019 CEPSR

Office hours: MW 4:00 - 5:00 PM

Texts: None. Handouts as needed.

TA: Jon Lederman; e-mail: jon@cisl.columbia.edu

Class webpage: http://www.cisl.columbia.edu/courses/spring-2000/ee4332/

Labs:

- VLSI Design Teaching Laboratory. 1212 Mudd Building. This lab is equipped with seven SUN workstations (sparta, delphi, rhodes, argos, thebes, corinth, athens, all at vlsi.columbia.edu). All of the CAD tools for the chip design will run on these machines. This course will make extensive use of industry-standard CAD tools from Cadence, Synopsys, and Avant!. The target technology for this course is a (reasonably) state-of-the-art 0.25µm, five-level-metal process from TSMC.

- Hardware Prototype Laboratory. 1211 Mudd Building. This lab has four PCs and ADSP-2181 demo boards for the MP3 software development. Eventually, when the chip comes back, a handful of students will be able to test and bring up the system in this lab in Fall, 2000.