• Complete the logic verification and synthesis. (Approximate check-point date: 3/22)

• Complete the detailed place-and-route. (Approximate check-point date: 4/10)
Columbia University  
Department of Electrical Engineering  
EE E4332, Spring, 2000  
Memory/host interface group work items

General comments: Your group is responsible for the design of the interfaces to external memory and the parallel-port host interface (which will be used to download music). For the parallel port, we will use hardware to manage the handshaking for the reading and writing of a single byte. The rest should be done in software. I have put a pointer to a description of the EPP protocol on the class web page.

For the memory interface, we are interfacing with several things:

- one or two off-chip SRAMs for “overflow” of the on-chip program and data memory
- a Flash memory which contains all the code. When the chip is reset, it automatically loads the contents of the Flash into the program memory.
- The SmartMedia card, which is handled like an I/O device

I have but some of the datasheets for this onto the class webpage. You will need to define some memory-mapped registers readable and writable by software that contain status, read/write addresses and data. You may also need to have counters to counter down the number of stall cycles for the external memory accesses.

I would also like this group to define and manage the memory-mapped “switch register,” the set of front-panel switches which software will poll (along with the parallel port) to determine things like “play”, “stop”, “advance”.

Your work items are:

- Decide on the “memory-interface” and “parallel-port” logic and your interface to the i-unit logic and the chip I/O. (Approximate check-point date: 2/18)

- Create a initial VHDL specification of your logic and a preliminary area estimate from synthesis. (Approximate check-point date: 3/1)