• RC interconnect modelling
• Driving large capacitive load, reducing RC delays

Structured layout design (2 Lectures)
Reading assignment: Rabaey, Appendix E
• Structured bitslice layout
• Standard-cell layout
• Chip layout and floorplanning
• Array layout

Other implementation issues (2 Lectures)
• Design for testability
• Packaging technology
• I/O issues: ESD protection, boundary scan, inductance, synchronization

Mini-design project due: 12/8
Final exam
Midterm: October 20.

Datapath functional units (2 Lectures)
Reading assignment: Rabaey, Chapter 7

- Adders
- Shifters
- Multipliers

Control logic strategies (2 Lectures)
Reading assignment: Rabaey, 10.6.1, 11.4-11.5

- PLAs
- Multi-level logic implementations
- Synthesis and place-and-route CAD

MOS memories (2 Lectures)
Reading assignment: Rabaey, Chapter 10

- Register files
- SRAM
- DRAM

Global interconnect modelling (2 Lectures)
Reading assignment: Rabaey, Chapter 8

- Capacitance, resistance, and inductance of interconnect
- Signal and power-supply integrity issues
- Electromigration
What makes a good logic gate?
Voltage transfer characteristic (dc behavior)
Switching behavior
Noise margins and power dissipation

Static and dynamic CMOS combinational logic gate, capacitance, and switch-level modelling (3 Lectures)
Reading assignment: Rabaey, Chapter 4
- Transistor sizing in static CMOS, logical effort
- Pass-transistor logic, sizing issues in pass-transistor design
- Domino logic gates
- Rules of thumb for estimating load capacitance
- Simple delay models (RC) for CMOS gates
- Power consumption
- Switch-level simulation models

Latches and clocking (3 Lectures)
Reading assignment: Rabaey, Chapter 6, 9.1
- Flip-flops versus latches
- Set-up and hold tests
- Static and dynamic latch and flip-flop circuits
- Clock design and clock skew
- Pulse-mode clocking, two-phase clocking
- Static timing analysis
• Challenges of VLSI design: power, timing, area, noise, testability, reliability and yield

• CAD tools: simulation, layout, synthesis, test, data management

Semiconductor device physics and MOS modelling (2 Lectures)
Reading assignment: Rabaey, 2.1-2.3

• pn junction models
• MOS device models
• MOS capacitors
• Short-channel effects and velocity saturation
• Introduction to BSIM3v3 device models
• Scaling of MOS circuits

Fabrication and layout (3 Lectures)
Reading assignment: Rabaey, Appendix A

• VLSI fabrication technology
• Layout view
• Layout CAD tools, Cadence Virtuoso, and the SCMOS layers
• Design rules: resolution rules and alignment rules
• MOSIS SCMOS design rules, and learning to read a design manual
• Stick diagrams, layout planning, and size estimation

The CMOS inverter (2 Lectures)
Reading assignment: Rabaey, 3.1-3.3, 3.5
The following books, which you might find useful as references, are on reserve in the Engineering Library:

- Glasser and Dobberpuhl, *The Design and Analysis of VLSI Circuits*, Addison-Wesley.
- Sutherland, Sproull, and Harris, *Logical effort: designing fast CMOS circuits*, Morgan Kaufmann.

**Grading:**

- Problem Sets: 20%
- Midterm: 20%
- Mini-design project: 20%
- Final Exam: 40%

**Topics**

Introduction to VLSI Design (1 Lecture)
Reading assignment: Rabaey, Chapter 1

- History of integrated circuits and technology scaling
- Levels of abstraction and the complexity of design

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Columbia University
Department of Electrical Engineering
Fall, 1999

Course: EE E4321, VLSI Circuits.

Instructor: Ken Shepard

E-mail: shepard@ee.columbia.edu

Office: 1019 CEPSR

Office hours: MW 4:00 - 5:00 PM


Class webpage: http://www.vlsi.columbia.edu/ee4321

Lab: VLSI Design Teaching Laboratory, 1212 Mudd Building. This course will make use of industry-standard CAD tools from Cadence and Avant!, supported for this course on the SPARC Solaris platform:

- Cadence Composer for schematic entry
- Cadence Virtuoso for layout design
- Avant! HSPICE for circuit simulation
- Cadence DIVA for layout verification and extraction.

The target technology for this course is an HP three-level-metal 0.5μm process (CMOS14), the same technology that is used in EE E4332 for those continuing to this course in the spring.

References: