• Carry-bypass adder
• Carry-select adder
• Carry-lookahead adder
• Tree adders

Shifters
• Barrel shifter
• Logarithmic shifter

Interconnect issues
• Scaling issues for R and C
• Elmore delay
• Pi-model, pole-residue macromodels and AWE analysis; moment matching
• Ceff modelling

Arrays
• ROMs: NOR- and NAND-based
• SRAMs: 6-T well, read, write, and decode circuitry
• PLAs: two-level logic optimization, static and dynamic PLAs

Misc topics
• Power analysis
• Design for testability
• Chip I/O
• Sizing issues for delay optimization: logical effort
• Power dissipation in static CMOS gates
• Pass-transistor circuits: 6-T XOR, pass-transistor multiplexers

Clocking and latches
• Flip-flops versus latches
• Static versus dynamic latches
• Latch circuits, true-single-phase clocking latches
• Two-phase clocking discipline; timing verification with two-phase clocking
• FSM design

Domino logic
• Basic domino gate in two-phase clocking discipline
• Noise issues in domino logic
• Sizing of domino logic
• Monotonicity requirement; timing requirements
• Delayed-reset domino and zipper domino

Adders
• Ripple carry adder: mirror full-adder cell, sizing, “dual” trick for fast implementation, typical tiling diagram
• Dynamic ripple-carry adder: Manchester carry chain, typical tiling diagram
Semiconductor device physics and MOS modelling

- Basic band structure, electrons and holes, doping
- pn junctions, junction electrostatics, and junction capacitance
- Basic MOS structure, MOS band diagrams
- MOS capacitor basics: inversion, accumulation, depletion
- Threshold voltage calculation
- Derivation of IV equations including velocity saturation effects
- Short and narrow-channel effects, DIBL
- Subthreshold leakage and its $V_{GS}$ and $T$ dependence

Fabrication and layout

- Basic CMOS processing steps and how they correspond to the layout layers used in design
- Design rules and their motivation
- Stick diagrams and estimating layout area from stick diagrams
- Layout-dependent device models

Static CMOS logic gates

- Voltage transfer characteristics
- Static dc noise margins
- RC switch model for static CMOS gates, including stacks