at \( A, B, \) and \( C \) between the “exact” extracted circuit (all the R’s and C’s) and the pi-model, Elmore delay model. Use a 100 \( psec \) slew time for the input to the driving inverter.

This problem is part of your final design project and should be done with your project partner.

2. You need to design the memory for your final design project. Your memory stores 8 8-bit (one-byte) words and has the following interface to the rest of your core:

Please precharge your memory with \( \phi_2 \) and qualify both the wordline and the write with the \( \phi_1 \) clock. Use the \( \text{mem\_read} \) signal to tristate the read driver. Only one level of decoding should be necessary (no predecoder). You are free to use the SRAM layout found in the cell \text{sramcell} in the library \text{arrayLib} in /u1/ee4321/arrayLib.

To complete your memory design, I expect:

- Sized schematics

- Layout of your memory design (remember to begin by making a tiling diagram and then stick layouts of your cells)

- HSPICE results for the read and write delays of your SRAM. Verify that reads do not disturb the contents of the cells and that you will always be able to write your cell.

- Use IRSIM to verify functionality for a larger number of patterns.
Columbia University  
Department of Electrical Engineering  
EE E4321. Problem Set #8. Memory design.  
Due: December 6, 1999

1. Consider the net shown in the figure below. The net is driven at $A$ and fanouts out to receivers $B$ and $C$. Each receiver has a load of $50 \, \text{fF}$. Assume that the wire is $0.4 \, \mu\text{m}$ wide and has a resistance of $0.076 \Omega/\text{square}$ and a capacitance (all to ground) of $0.1 \, \text{fF}/\mu\text{m}$. Use a lumped approximation of this distributed system (new R every 100 squares, say).

(a) Find the Elmore delay to each of the receivers $B$ and $C$.

(b) Find the pi-model at $A$ that approximates the load of the wire (and fanout). Comment on the amount of resistive shielding of the load. (*Hint:* To find the pi-model, you will need to calculate the moments of the admittance at $A$. You might find MATLAB helpful for this, which is available on the SUNs by typing `matlab`. I am assuming that you all have some familiarity with MATLAB. If not, please see me or the TA for additional help.)

(c) Assume that the driver at $A$ is a CMOS14TB inverter with $W_p = 20 \mu\text{m}$ and $W_n = 10 \mu\text{m}$. Compare the HSPICE results you obtain for the waveforms