Volume 10
Number 1
January 2005

SOLID-STATE CIRCUITS

IEEE Solid-State Circuits Society Quarterly Newsletter

ISSCC Enters the Nanoelectronic Integrated-Circuit Era

ISSCC 2005 in San Francisco, California, 6–10 February, the foremost global forum for new developments in the integrated-circuit industry, will feature the theme "Entering the nanoelectronic integrated-circuit era." With the appearance of integrated circuits having transistor dimensions less than 100 nm, integrated circuit technology is moving from the microelectronic era into the nanoelectronic era. Three Plenary Session speakers will launch the three-day conference with their comments and views on the challenges ahead.

this IN issue

Daeje Chin, Korea's Minister of Information and Communications, will address the registrants on "Nanoelectronics for the ubiquitous information society." Chin holds that the economic risk to develop process technology for manufacturing nanodevice parameters will require the government to play a key role. Tight collaboration among semiconductor manufacturers, system infrastructure providers, and service industries will be essential.

Hugo De Man, a senior research Fellow at IMEC and a professor at Katholieke Universiteit Leuven, Belgium, will talk about "Ambient intelligence: gigascale dreams and nanoscale realities." The future will require two-orders-of-magnitude-lower power dissipation than today's processors, at one-twentieth the cost. Breakthroughs will have to be achieved in nanoscale-device quantum physics, in parameter-variation control at the atomic level, and in low-power software at the top of the product-development chain. De Man will address the physical realities of devices and interconnects at the nanoscale level, such as gate and source-drain leakage, and transistor-parameter variability. "More-than-Moore" improvements in transistor density will be required, such as MEMS structures and new materials and devices for sensors and wireless sensor networks.

Sunlin Chou, Senior Vice President and General Manager, Technology and Manufacturing Group, Intel, Hillsboro, Oregon, will speak on "Innovation and integration in the nanoelectronics era." With transistors and circuit elements already at nanoscale dimensions, Chou asserts that innovation will accelerate through skillful integration of new materials, processes, and device structures. Hardware and software are already evolving solutions via multitasking, parallel processing, mobility, and wireless connectivity. Likewise efficient use of power in nanoelectronics will call for holistic solutions involving systems, circuits, processes, devices, and packaging. Chou concludes that innovation and integration of nanotechnology will extend Moore's Law beyond the next decade.

During the three central days of the conference, 233 technical papers will be presented in thirty-one sessions. Papers covering wireless topics continue to lead the technical coverage of ISSCC at 18%, with analog and wireline topics running right behind at 16% each. The other five topics are listed in the order of technical coverage at the conference. What follows are selected highlights of the eight major topics of the conference.

Registration for tutorials, forums, and short courses fill up quickly. Please see the offerings online and register at *www.isscc.org/isscc*.

Wireless Communications

In Session 5, Atheros and Broadcom will present the most integrated solutions to date on CMOS WiFi-on-a-chip. With many architectures to

Continued on page 2

SSCS Elects Five AdCom Members page 10

Continued from page 1

achieve a CMOS WLAN system, Atheros utilizes a sliding-IF super-heterodyne structure, which eliminates one of the on-chip phase-locked loops required in traditional super-heterodyne radios. The Broadcom SOC has an antenna as its input and digital bits (to the host processor) as its output.

Due to the radically different signaling technique of WiFi from ultra wide band (UWB), developers face the challenge that no fully-integrated UWB transceivers exist today. Session 11 contributors will present concept circuits. One example of encouraging performance will be presented by developers from the California Institute of Technology, who solved propagation challenges at 24 GHz by applying radar technology or a phased array multiple-antenna system on both the receiver and the transmitter. The beamforming function of the chip can also be used for ranging and sensing applications, effectively making it the world's first radar-on-a-chip.

During Session 17, Berkana Wireless will showcase, for the first time, the technology of a fully-integrated quad-band GSM transceiver in mature low-cost 0.18-µm CMOS. This design has the best sensitivity/linearity and power dissipation tradeoff on the market today for CMOS transceivers, showing that we are one step closer to low-cost single-chip cell phones.

New applications for silicon-based IC technologies that are in the process of being defined in frequency bands well above 10 GHz will be presented in Session 29. Developers from the University of Toronto, Delft University of Technology, and IBM will describe the first SiGe power amplifier to deliver more than 100 mW at 26 GHz, five times higher than prior art. The amplifier has 20-dB gain and a good efficiency (more than 12.5%). To achieve this, metal layers in the technology (that are normally used for connecting transistors) are stacked to form transformers.

Developers from Broadband will present a noise-cancellation technique in active RF-CMOS mixers. MOS transistors have much higher flicker noise than BJT transistors. The novel technique steers away the flicker-noise current at brief intervals within the signal waveform. This results in a dramatic improvement (ten times) in noise performance for a direct-conversion mixer, with no penalty in power consumption, chip area, gain, or linearity.

Wireline Communications

In Session 3, two of the backplanes that will be presented double the bit rate from existing 3-Gb/s (XAUI) to 6-Gb/s backplanes. The increasing clock rates of processing cores that accompany the continuing advances in silicon technology drive the need for higher-speed electrical interconnects. In separate papers, IBM and Texas Instruments each will present backplanes that employ feed-forward equalization and decision-feedback equalization. This combination optimally compensates for bandwidth losses and provides improved immunity to intersymbol interference (ISI) and crosstalk.

In Session 8 Seoul National University will describe judicious use of circuit techniques to enable a 40-Gb/s transmitter out of 0.13-µm CMOS. The single-chip 40-Gb/s transmitter runs an onboard 20-GHz PLL, a 16:1 MUX, and a PRBS generator, achieving power consumption of just 2.8 W.

Session 12 will address the optical communications benefits from low-power and low-voltage laser drivers and high-speed and low-power burst mode receivers. Analog Devices developers will present a 10-Gb/s laser driver with

impedance-matched electrical output, delivering all of the signal power to the laser diode and enabling the use of cheaper packaging for the laser.

During Session 18, high-speed interconnects and techniques to overcome the non-idealities of the transmission channels will be addressed. Borrowing from wireless-circuit architectures based on modulation techniques for enhanced broadband performance provides advantages. Developers from SST Communications and UCLA will describe a technique that modulates the transmitted data signal to create two independent high-speed channels. This circuit, realized in 0.18-µm CMOS, achieves an aggregate data rate of up to 3.6-Gb/s per pin, and dissipates 92 mW.

Session 22 will include near-ideal multi-Gb/s clocks that permit higher data rates over both new and existing links, and enable greater transmission distances. IBM and Miromico developers will present a multiple-clock-phase PLL with dedicated phase detectors that permit sub-ps rms tracking jitter at 10 Gb/s. Synopsis will present special circuit techniques and address loop dynamics to enable a lower-power small-area PLL with 1.3-ps rms jitter at 3.125 GHz.

Analog

A key element in the signal chain, the digital-to-analog converter (DAC), will be the focus of Session 6. A DAC with clock rates up to 22 gigasamples per second will be presented by Nortel Networks and Institut fuer Mikroelektronik—that is over twice as fast as any 6-b design previously published. Another direct synthesis of multicarrier signals at higher IF and an important step towards 'software radio' will be presented by Philips and Technical University Eindhoven. Using a minimum-complexity circuit-design approach and conventional CMOS architecture, the DAC performs 500 MS/s.

Session 9 will feature major developments in the design and realization of A/D converters. Developers from Oregon State University and Asahi Kasei Microsystems used a switched-RC integrator technique to enable the operation of the ΔΣM at 0.6 V. This is accomplished without any clockboosting, bootstrapping, or switched-opamp techniques. A feed-forward topology to reduce the dynamic range at the integrator output node also enables the low-voltage operation and 1-mW power consumption.

Session 15 will focus on ADCs with speeds ranging from 1 MS/s to 200 MS/s, and resolution ranges from 16-b to 8-b, enabled by dynamic voltage management. The University of Toronto and Texas Instruments will present a 90-nm digital CMOS pipelined 10-b ADC that operates from a 1.2-V supply, achieving a peak SNDR of 52.6 dB, 12MS/s, while consuming 3.3 mW of power.

Session 27 will focus on filters and continuous-time ΔΣ converters. CT noise-shaping can yield valuable savings in power, and can also provide useful attenuation of interference before the first sampling function. The University of Toronto uses an improved complex noise shaper to attain a single-sided bandwidth of 23 MHz. The 72.5-dB dynamic range and 45-dB image rejection for only 42.5 mW permits direct digitization in a low-IF WLAN receiver with minimal additional analog functions. Columbia University will show that useful self-tuning filters can be realized at extremely low voltages without resorting to special device thresholds. Employing a new transconductor design with body bias tuning, the 135-kHz filter achieves a DR of 57 dB with only a 0.5-V supply.

Digital

In Session 10, all eight papers will describe microprocessors containing multiple processor cores of various types rather than higher frequencies. New approaches to dynamic voltage and frequency scaling to reduce power consumption will be discussed in this session.

Implementation of a next-generation Itanium® processor will be described by Hewlett-Packard and Intel. It is comprised of two dual-threaded cores integrated on the same die with a 26.5-MB cache in 90 nm. In addition to performance improvements, this design reduces susceptibility to soft errors and improves power efficiency through low-power techniques and active power management.

The first-generation multicore SOC CELL processor, to be described by IBM, Sony, and Toshiba, combines eight streaming processors on a chip providing a high-performance platform for multimedia and streaming workloads. These processors are designed with features specifically targeted for certain applications, saving power and area by this narrower application focus. Implemented in a 90-nm SOI process, the chip incorporates extensive power- and thermal-management techniques.

The processor that will be described by Sun Microsystems also follows the dual-core approach to improving performance through parallelism. This fourth-generation SPARC® processor combines two enhanced third-generation cores with expanded caches and an on-chip 2-MB L2 cache. Fabricated in a 90-nm technology, it operates at 1.8 GHz from a 1.1-V supply.

Another approach, which will be described by IBM (BlueGene/L), uses low-cost, small, power-efficient processors in a massively parallel fashion. This complex SOC ASIC includes two processor cores, embedded DRAM, SRAM, and custom logic, achieving a high-power/cost-performance trade-off, suited to its role as a building block of IBM's BlueGene/L supercomputer.

For on-chip interconnection the University of Twente and Philips will propose a differential-signaling scheme as an alternative to classic repeater-based wiring in Session 20.

Developers from Rambus and Stanford University will address the transfer of data on and off chip at the high intrinsic speed of advanced processors. They will pre-

sent an I/O interface with a total data rate of more than 0.5 terabits/second (that is, 500 billion bits per second)! Each pin operates at a data rate of 6.4 Gb/s, consuming an energy of only 20 pJ for every transferred bit. To achieve an accurate timing relationship between the I/O pins, the presenters will describe the on-chip clock-distribution technique that delivers the reference clock across the width of the I/O interface with a clock-tracking architecture that allows the use of low-cost clock sources. These circuits can maintain high analog performance even in an SOI CMOS process.

Technology Directions

Session 4 will feature hybrid interdisciplinary technologies that demonstrate exciting and powerful new integration directions.

The Max Planck Institute will explain a true breakthrough, a neuron-cell-to-semiconductor connection that enables neuroelectronic communication, an exchange that is noninvasive for the cells and noncorrosive for the chips, using purely capacitive effects across the interface. Information is transmitted in electronic systems by electrons and in neurons by ions. Being able to achieve information exchange between these two different charge carriers is a significant challenge. Such microscopic interfacing is demonstrated between a silicon chip and snail neurons, with the diameter of the interface junction estimated to be between 10 and 100 microns.

The University of Michigan will discuss a miniaturized microsystem for an atomic clock with the accurate timing needed for electronic communication systems, such as the Global-Positioning System (GPS). With MEMS realization of the atomic-clock package with a sealed cesium-vapor cell, and integration of other components, the fabricated device is smaller than a sugar cube, and consumes only 30 mW of power. The result is 700 times smaller than the present art.

Developers from IMEC, ASM, IMSE-CNM, Philips, and Bosch will discuss a MEMS gyroscope integrated on top of a CMOS wafer. The combination performs both directional sensing and information processing. This implies that the MEMS must be made at sufficiently low temperatures (below 400°C), so that the underlying CMOS is not degraded. Integration of sensing and processing makes this the world's first single-chip miniature-gyroscope solution having excellent performance.

Session 14 will look at low-power wireless and advanced integration. CSEM, Xemics, and Texas Instruments will present an ultra-low-power demonstration of sensor integration using a radio electronic interface. This type of solution can be used for distributed sensing applications because of the ultra-low-power integrated-sensor node.

Developers from Keio University and the University of Tokyo will present 1-terabit/s wireless communication among chips in a package, especially useful for three-dimensional integration schemes. The transmit power-control scheme eliminates interference and optimizes power dissipation.

Session 21 will look at the 60-GHz frequency band, once the exclusive domain of III-V-compound semiconductors, such as GaAs and InP. However, aggressive scaling of CMOS technology is making possible the fabrication of high-data-rate wireless communications for home, office, or automotive anti-collision warning systems. Researchers at National Taiwan University offer, for the first time, two essential building blocks (a VCO and broadband amplifier) for creating a robust 60-GHz radio in conventional CMOS technology. The VCO is operational at a much higher frequency (to 114 GHz). UCLA will present a low-noise amplifier and a mixer for frequency translation directly to DC, each for use in a 60-GHz receiver.

Among the presentations on advanced array structures in Session 32 will be organic transistors integrated into a flexible scanner and display. Researchers from the University of Tokyo will describe a new circuit concept called 'double word-line and bit-line structure' that dramatically reduces the delay of the circuit by a factor of five, and the power by a factor of seven. In order to realize the new structure, two layers of organic transistors are stacked in three dimensions, for the first time, together with organic photodetectors, using laser drilling. The resulting faster circuit has enabled a sheet-type scanner made with flexible plastic sheets. This portable, ultra-lightweight and flexible scanner is made possible by organic-transistor technology. A prototype of the sheet-type scanner is less than one millimeter thick, with an area of eight square centimeters, with 64 x 64 resolution. If four million pixels were to be implemented in a future design, the time for a single scan is estimated to be less than one minute using these 3-D organic circuits.

Signal Processing

National Taiwan University will report in Session 7, the first implementation of a high-definition single-chip H.264 video encoder. This standard has features that will enable the possible presentation of high-definition digital-video disc (HD-DVD) and digital-video broadcasting on handheld terminals (DVB-H), a considerable improvement on MPEG-2 and MPEG-4. The encoder contains a main controller and five engines for integer motion estimation (IME), fractional motion estimation (FME), intra-prediction (IP), entropy coding (EC), and deblocking (DB). The core size of the chip is 31.72 square millimeters using 0.18-micron CMOS technology. It contains 923-K logic gates and 35-KB SRAM. Power dissipation is 581 mW for D1 video (YUV420, 720x480, 30 fps), and is 785 mW for HDTV 720p video.

Two designs that will be presented in Session 24 are among the fastest and lowest-power UWB transceivers reported to date. While one transceiver pursues an aggres-

sive data rate, the other focuses on ultra-low power consumption.

The first solution from National Chiao Tung University implements a high-data-rate 480-Mb/s UWB baseband transceiver based on coded multicarrier techniques. This design consumes a total power of 575 mW, providing an energy efficiency of 1.2 nJ/bit. The second design from National Taiwan University implements a 62.5-Mb/s UWB transceiver, which consumes only 6.7 mW, and occupies an area of under 3 square millimeters in 0.18-micron CMOS technology. This corresponds to an impressive energy efficiency of 0.1 nJ/bit!

Two recent innovations in WLAN baseband transceivers that improve the reliability of wireless channels and increase the coverage area of existing WLANs will be presented in Session 24.

Atheros will describe its multi-antenna solution, which utilizes advanced signal-processing techniques to greatly increase the reliability and range of conventional WLAN channels. Atheros will also describe its advanced packet-management functions, which facilitate video transmission. In the enterprise arena, the wide range of data rates used within the same channel results in low-rate clients, severely limiting the performance of high-rate clients, yielding low overall network performance.

Engim will describe a wideband WLAN solution that is capable of operating on three adjacent channels concurrently. This wideband multichannel approach allows low-rate clients to be grouped on a slow channel, while high-rate clients can operate unimpeded on a fast channel, yielding much better overall network performance. Engim will also discuss its real-time spectral-monitoring facilities that provide advanced network-management capabilities to detect interferers and rogue clients, allowing for improved performance and security.

Imagers, MEMS, and Displays

In Session 13, Delft University of Technology will present a low-cost CMOS temperature sensor that achieves accuracy of ±0.1°C over the temperature range of –55°C to 125°C. This 4.5 mm² chip offers a fivefold improvement over former art using microwatts of power, which makes it ideal for low-cost wireless-sensor networks. The Universities of Michigan and Utah, along with Analog Devices, will present a CMOS micro-sensor that can detect less than 1 ppb of lead concentration, fabricated by using a few thin-film post processing steps.

In Session 19, Sanyo Electric will present the smallest pixel yet, 1.56-µm x 1.56-µm pixels with 7-V operation. The smaller pixels in this CCD imager improve the image-resolution-to-cost tradeoff. This design significantly reduces smear to –75 dB by using a 9-phase vertical-transfer technique. MIT Lincoln Laboratories will demonstrate a one-megapixel image sensor with processing behind every pixel by advancements in fabrication processing; wafer bonding with small 2-µm x 2-µm x 7.5-µm 3D vias.

In Session 30, Sandia National Labs and the University of Michigan will describe how they have improved the monitoring of analog information systems that feed a huge amount of data while only a small portion of transferred data carries relevant information. Through spike detection that recognizes relevant events only, they reduce data for real-time processing by eliminating 92% of the bottlenecks.

Memory

Two papers that will be presented in Session 2 exhibit the highest-density flash memories ever reported: 8 Gb fabricated in advanced 70-nm (Toshiba and SanDisk) and 63-nm (Samsung) technologies, using a multi-level approach and NAND structure. Write performance is dramatically improved to reach a level comparable with single-bit-per-cell memories.

Intel will present the fastest synchronous-read frequency and programming throughput ever reported with a 512-Mb flash memory in 90-nm technology. It is targeted at communications and multimedia applications that demand both fast code execution and fast nonvolatile data storage. The memory is capable of a 166-MHz continuous-burst mode for fast code execution. Concurrent 166-MHz read operation and 1.5-MB/s programming operation is offered for memory subsystems that require simultaneous read and write operations.

In Session 25, Matsushita Electric Industrial will present the fastest random-cycle embedded DRAM. The 400-MHz 1.5-V dual-port interleaved DRAM has been developed with only two key additions to a 0.15-µm CMOS logic process: sense-signal-loss-compensating technology, based on an intensely-detailed noise-element analysis, and a striped-trench capacitor (STC) cell that is fabricated by adding only one mask.

Samsung will present the first commercially-viable 2-Gb DRAM. By the creative use of a third level of metal (typically not found in DRAMs), and an unconventional bank arrangement, Samsung memory developers have been able to modify the chip-aspect ratio to fit the JEDEC industry-standard packaging.

In Session 26, Samsung will introduce the world's largest SRAM at 256 Mb. Based on their 0.16-µm² stacked single-crystal-silicon thin-film-transistor SRAM cell, introduced at the 2004 VLSI Symposium, the 256-Mb chip has an area of just 61.1 mm². The novel design approach uses the stacked single-crystal-silicon thin-film transistor as the local column-select transistor in a hierarchical bitline architecture, to virtually eliminate the usual area penalty associated with this approach. An array efficiency of over 70% is achieved, while maintaining the power and speed benefits of the short hierarchical bitlines. The chip is ideally suited for mobile applications, opening this low-power market to the benefits of very-high-density, high-bandwidth static memory.

Hewlett Packard and Intel will present a three-times increase in the Itanium L3 cache size. The 24-MB

L3 cache is the largest embedded memory ever reported. Thanks to improvements in array design, and a reduced array of operating voltage, the L3 cache consumes only 4.2 W, with cache latency reduced from eight cycles to five. A shift from the traditional synchronous-SRAM design approach to an asynchronous design also eliminates clocking power in the memory arrays.

Details Online

Forums and Short Courses are scheduled for the first and last days of the conference. To register, or for a more detailed view of all the presentations in the Advance Program, go to *www.isscc.org/isscc*. Articles from the ISSCC 2005 Digest will be available in IEEE *Xplore*™ by summer.

Anne O'Neill
SSCS Executive Director
a.oneill@ieee.org

A *JSSC* Classic Paper: Matching Properties of MOS Transistors

Published in the October 1989 *JSSC*, "Matching properties of MOS transistors" by Marcel J.M. Pelgrom, Aad C.J. Duinmaijer, and Anton P.G. Welbers of Phillips Research Laboratories, Eindhoven, Netherlands, is a classic article. It has been cited more than 150 times according the Journal Citation Report, 2003 Science Edition. The concepts were presented first in the fall meeting of ESSCIRC one year before they were published in the *JSSC*.

Background

Around the year 1980 a major project in Philips Research Laboratories aimed at digitizing the television system. An essential part of this project was a video-field store, which had a 2.4-Mbit size. It was a ridiculously small memory from today's perspective. However, in an era when people were struggling with expensive 16-kbit DRAMs, realizing a cheap video-field store of this size was a real breakthrough.

In the design phase of this memory a significant area reduction could be achieved by rotating one of the sense amp transistors by 90°. The potential hazard was in spending too much on guarding headroom for the unknown amount of mismatch this rotation would introduce. So a small test circuit was designed in a 2- m NMOS enhancement-depletion process to find out the consequences of this rotation.

In that same period matching of IC components was already an important subject: the introduction of the CD audio format required digital-to-analog converters with resolutions of 14 to 16 bits. Matching was related to analog, and analog was equivalent to bipolar technology, so everybody knew for many years that the lithographical precision of the emitter caused the mismatch.

The first NMOS measurements (1982–83), however, did not meet those emitter lithography assumptions and showed many more effects that pointed in other directions. In addition to the lack of a decent model, setting up an accurate automated test system was a major struggle. The third test set-up finally showed sufficient accuracy and repeatability of the measurements to start a large-scale characterization. With correct data, the observation of the relationship with the inverse square of the area was not too difficult. From there the theoretical search for the underlying charge-related mechanisms could start.

Publishing the Results

We gained more and more confidence in the theoretical basis we were building up because we had access to the early process generations of a large company. Also, we had a test set-up that would run throughout the weekend when there were fewer noise sources, which provided results of great sensitivity. The simple model provided the means to analyze yield, and consequently many other effects came to the surface. In 1986 Lakshmikumar published his measurements, which fit well with the results from the corresponding Philips technology. (Kadabar R.Lakshmikumar, Robert A. Hadaway, and Miles A. Copeland published "Characterization and modeling of mismatch in MOS transistors for precision analog design" in the December 1986 *JSSC*, another often-cited *JSSC* classic article.) This was another indication that the often-heard statement, "mismatch was a production-plant-specific issue," needed revision.

In some four-to-five years many hundred thousands of devices on wafers in various process generations were measured. This allowed refining the model and confirming the oxide thickness scaling. Designs with yield problems were analyzed and predictions of redesign measurements turned out to be valuable.

The first conference publication of the matching work was in ESSCIRC 1988, followed by the submission of the paper to the *Journal of Solid-State Circuits*. However, the manuscript almost did not get

accepted. Both reviewers were pretty critical. The first one said that the "paper might be better off by just presenting experimental data without many equations," while the second stated that "the analysis of mismatch in the Fourier transform domain contributes new insight … its neglect of the underlying physical mechanisms leaves several questions unanswered." Publication as a correspondence item was recommended. With one reviewer in favor of the theory and the other in favor of the experimental data, the associate editor at the time, Charles Sodini, allowed a full paper. So, do not despair if you receive a (very) critical review; you still might end up high on this list.

Follow-up

It still took some five years before the paper started appearing in reference lists. In the mid-1990s technology had reached a point where it became commercially attractive to integrate analog functions on a CMOS chip (system-on-chip). This trend made the matching problem more visible to industry. The one-parameter mathematical description (A_{VT}) allowed easy communication on the matching properties between designers and technologists; foundries started quoting the A_{VT} matching coefficient in their process descriptions. A_{VT} is the mismatch constant equal to the standard deviation between the threshold voltages of a pair of transistors, each sized 1 square micron. Other transistor dimensions are easily derived by dividing A_{VT} by the square root of their area.

Moreover, designers realized that the right balance between (analog) yield and electrical performance would give them a competitive edge. The paper predicted the matching behavior in future process generations by linking the matching coefficient to the gate-oxide thickness. This prediction has turned out to be largely valid, even for today's processes.

The characterization groups, realizing that this phenomenon was a lasting design constraint, now started measuring matching characteristics. So, once started as a designer's problem, matching became a technologist's concern. Process people realized the value of monitoring the mismatch behavior, as it often served as an early warning indicator for yield problems. In advanced processes the consequences of certain technological steps on matching performance are well understood, and therefore matching plays a role in the entire technology architecture.

Many researchers from academia and industry have been studying mismatch over the last ten years. Valuable papers have been written on subthreshold extension of the model, as well as application of the idea to bipolar mismatch. Many technology artifacts influencing matching were identified and published in *IEDM* and *ICMTS*. People have tried to refine the model; however, improving the significance of any statistical prediction is very difficult. On one hand, the model already covers all area-related mechanisms. On the other hand, it requires measuring many ten thousands of devices to determine the second digit of the standard deviation with sufficient relevance.

Still there remains some truth in the second reviewer's remark; some of the basic physical mechanisms have not yet been thoroughly analyzed. The fundamentals behind the mismatch issues in the current factor are still hidden and, perhaps, will reveal new insights.

Outlook

As dimensions shrink, the granularity of the silicon device will play a more and more dominant role. In a 0.25- m process the behavior of the minimum-size device was determined by some 1200 doping atoms, at the 65-nm node there are only 80–100 atoms that play a role. The influence of the uncertainty increases to a level such that even standard digital CMOS circuit designers have to take mismatch into account. Where in the analog world mismatch can be circumvented by choosing optimum architectures and elaborate calibration schemes, there seems to be little room for improvement in standard digital cells. A potential improvement in matching may come from new device structure where dual gates control the current flow. However, also in these structures some granularity effects, caused by working with devices measuring a limited number lattice distances, will appear.

It seems inevitable that we are now entering an era where statistical design is the rule not the exception. The 1989 paper was perhaps a noticeable step in that direction. Yet we will see many more papers exploring the statistical behavior of the devices and their interaction with technology. The ways to predict these effects in simulations are still in their infancy and, on a system level, only the first steps have been taken to deal with these problems.

And the video memories? They were produced and designed into the first digital televisions. These memories allowed television system designers to explore, implement, and test video-field-related processing. The original plan for digitizing television materialized many years later in a completely different form. That is the thrilling side of research; it will never deliver what you expect, but what it ultimately delivers is beyond your expectation!

Marcel Pelgrom
Scientist, Philips Research Lab, Eindhoven
marcel.pelgrom@philips.com

A *JSSC* Classic Paper:

Sigma-Delta Converters

Published in the December 1988 *JSSC*, ""The Design of Sigma-Delta Modulation Analog-to-Digital Converters," by Bernhard E. Boser and Bruce A. Wooley, is a classic article. It has been cited more than 100 times according the Journal Citation Report, 2003 Science Edition.

For more classic, often-cited articles from the *Journal of Solid-State Circuits* see the Web site *sscs.org/jssc/top-cites.htm*.

Bernhard Boser comments:

When I arrived at Stanford University in fall of 1984, Bruce Wooley just had joined the faculty. He introduced me to the topic of oversampled A/D conversion by handing me the draft of a now-famous paper on the topic by James Candy ("A use of double integration ..."). I must have read the paper at least ten times and still did not understand the thing. So I wrote a little program to check out the ideas and, low and behold, this thing WAS a converter. But how did it work?

It took me many months (more precisely, years) to answer this question. On the path there I met many engineers who flat-out stated that getting 16-bit accuracy out of what seemed to be just a 1-bit converter was plain impossible. I even found a doctoral thesis giving a 'proof' that higher-order modulators could not work!

In good engineering tradition I proved the skeptics wrong not with a piece of computer code but with an actually working silicon example. In designing that part I was faced with another set of questions: Only a 1-bit ADC (that is, a simple comparator) is needed, but what about its accuracy? Are the offset, hysteresis, and noise specifications at the 16-bit or 1-bit level? What about the requirements for the other components? By now well researched, these questions were most confusing in the mid-1980s.

When I got my sigma-delta modulator working I saw an opportunity to help the community by presenting my experiences and conclusions in writing so that others would not have to take my arduous (and rewarding!) path. I hope I succeeded in helping some readers grasp the concept of sigma-delta modulation a little more quickly than I did. Of course, the results presented in my article have long been exceeded, refined and extended.

I blush when I think that my paper also contains at least one inaccuracy when it states overly modest gain requirements for the amplifiers. Fortunately, engineers never stand still and much has been written on the topic since. Still, it is rewarding to see that authors still cite (and read?) my publication. It is a big honor to appear on the *Journal's* list of most-cited papers.

Bruce Wooley comments:

The invention of the transistor in the mid-20th century was followed by the rapid growth of interest in digitizing information for communications, storage and signal processing. In particular, attention began to focus on the use of digital transmission and switching in the voice telephone network. Analog-to-digital conversion thus became an increasingly important function in the communications infrastructure in both Europe and North America.

Prior to the emergence of large-scale MOS integrated circuits, A/D converters for applications in communications were typically expensive, rack-mounted systems that were shared among multiple channels in order to amortize their cost. However, the emergence of MOS VLSI technology and the ability to integrate thousands of digital gates on a silicon chip motivated efforts to find a means of exploiting this capability to reduce the cost of digitizing analog signals.

Oversampling approaches to digitizing analog signals, which combine sampling at well above the Nyquist rate with feedback and digital filtering, offer a means of exchanging resolution in time for that in amplitude. Thus, they are an effective approach for exploiting the component density and speed of scaled VLSI technology to avoid the need for complex, precision analog circuits.

Oversampling modulation for analog-to-digital conversion first appeared in the form of delta modulation, which was introduced at about the same time as the invention of the transistor. Ten years later an approach referred to as sigma-delta, or equivalently delta-sigma, modulation was introduced. As opposed to delta-modulators, which encode the rate of change of a signal, sigma-delta modulators digitize the signal itself while shaping the resulting quantization noise in frequency so as to push most of its energy outside the signal band where it can be removed by digital filtering. Consequently, they are an especially robust means of digitizing signals that require only a very limited amount of analog circuitry.

Bernhard's research focused on devising architectures and circuit implementations best suited to implementing precision A/D converters in scaled digital VLSI technologies. As described in the *JSSC* paper, his work focused on the design and realization of second-order sigma-delta modulators, which avoid the large spurious noise tones inherent in first-order architectures, as well as the stability concerns associated higher-order loops. He established

behavioral models for each of the functional building blocks in a second-order modulator that included the impairments associated with practical circuit realizations. Extensive simulations were then used to establish the circuit design criteria for each of these blocks, and an experimental modulator was integrated to verify the validity of these criteria.

Because the performance of oversampling modulators can only be assessed by examining long data traces, they cannot be efficiently simulated at the circuit level. As an alternative, Bernhard developed an event-driven functional simulator for mixed digital and analog sampled-data systems (MIDAS) to accomplish this task. This simulator was a critical component of Bernhard's research and is still in widespread use today.

The Impact

Noise-shaping modulators now play a dominant role in the realization of A/D converters, not only for voice telephony, but also in a broad range of digital audio systems. Moreover, they are beginning to make inroads into applications with higher bandwidths.

The papers resulting from Bernhard's work continue to serve as a foundational reference for insight into the simulation and design of noise-shaping oversampled A/D converters at both the architectural and circuit levels. His work clearly established the critical circuit requirements for designing such modulators, and it pointed the way to the effective modeling of such systems at the behavioral level. The second-order modulator design he proposed and demonstrated has subsequently served as the key building block for the realization of higher-order, cascaded sigma-delta modulators that have been used to digitize both low-pass and bandpass signals with bandwidths of several megahertz and center frequencies as high as 20 MHz. Moreover, the software he developed remains a valuable tool for assessing the behavior of mixed-signal systems in which feedback plays an important role.

SSCS e-News More Often in 2005; Less Paper

Beginning January 2005, SSCS e-News alerts will come in alternate months, six times a year instead of quarterly. In contrast, the print newsletter (for those who still receive the postal mailed version) will come less frequently, once every four months, or three times a year. Those receiving the e-News alerts will be given twice as much news on the Society's Web site as those dependent on the print version. The news site online will feature a new look and feel as well.

The print version will come January, May, and September, and will be timed to include information about major upcoming SSCS conferences (the ISSCC in February, the VLSI Symposium on Circuits in June and the CICC in October). Additional coverage in the expanded e-News postings will include more information about IEEE elections, IEEE Fellows, books of interest to members, technology highlights, reminders about nomination deadlines, and deadlines for best rates for advance registration for conferences.

E-News alerts to the bimonthly *SSCS Newsletter* are available free to SSCS members. If you aren't receiving the e-News alerts yet it's because your email address is not in the IEEE member database. Or you may have opted out of receiving the e-News alerts.

1. To update your member record online *www.ieee.org/emembership.manage.xml*
2. To request e-News delivery or opt out, use the online form at *sscs.org/e-enews*

E-News Serves Members' Interests

The move to email alerts of the *SSCS Newsletter* posted online is serving our members well since its launch in January 2003. Analysis of the hits to the Society electronic news for April and July 2004 shows that on the day that an email notice is mailed, there is a four- to fivefold increase in hits to the e-News site. There were twice as many visits and twice as many unique visitors during the issue month of April compared to July, perhaps because of summer vacations. But each visitor averaged more page views per visit in July, and spent longer at the site.

Articles that named people were the most frequently read articles, for example, "Ultra-wideband wirelsss chip wins student design contest," " *JSSC* Best Paper awarded to Shrivanik Su and Wooley," and "Nagaraj named new editor-in-chief for *JSSC*." Cover stories on the VLSI Circuits Symposium and CICC were next most read along with the table of contents of each issue. "Congratulations to new Senior Members" was among the top 10 articles for both issues and in April even had more hits than the 2004 class of IEEE Fellows. Older articles continue to be read: the January and April 2003 articles on the Gilbert cell, and the October 2003 review of the business bestseller *Good to Great: Why Some Companies Make the Leap and Others Don't.*

Newsletter coverage for 2005 will include more commentary on *JSSC* classics and coverage of books of interest.

SSCS Elects Five AdCom Members

Three new members will join the IEEE SSCS Administrative Committee when it meets 6 February 2005, and two incumbents will return. The SSCS membership elected new members Bill Biderman, Terri Fiez and Mehmet Soyuer last fall. David Johns and Takayasu Sakurai will return to serve three-year terms.

"Our congratulations go out to these leaders in their field," said Charlie Sodini, SSCS Past-President and Nominating Committee Chair, "and our gratitude for the willingness to serve of all the candidates. SSCS bylaws specify that we must provide our members a choice and with so many talented leaders, the choice is a difficult one."

The AdCom is responsible for overseeing conferences, publications, and other potential technical activities within the Society's field of interest. Each AdCom member serves a three-year term. Terms are staggered so there are always some experienced members and some new members. The Nominating Committee puts together a ballot of candidates each summer. A member can petition to be included on the ballot. See details online at sscs.org/nomelec.htm.

William R. Biderman (M'89) received his BS and MS degrees in electrical engineering and computer science from the Massachusetts Institute of Technology in 1978. Currently he is Vice President of Sensor Development at Pixim Inc., a Silicon Valley startup delivering high dynamic-range CMOS image sensors to the security market. He managed the Advanced Development Group at DEC, which produced a self-contained liquid-nitrogen-cooled computer system and the groundbreaking Alpha microprocessor. Over the past 20 years, Mr. Biderman contributed to the first VAX microprocessors, managed the first SPARC V9 implementation at HaL Computers, and led the development of a novel media-processor at Chromatic Research. He began his career at HP Labs, where he designed dynamic RAMs and EEPROM devices.

Mr. Biderman currently serves on the Executive Committee of the Symposia on VLSI Circuits and Technology (Treasurer) and has previously served as the General Chair ('99–'00), Program Chair ('97–'98) and as a Program Committee member since 1993. He twice has been a member of the ISSCC Program Committee and has edited several special editions of the *IEEE Journal of Solid-State Circuits*.

David A. Johns received his BASc, MASc, and PhD degrees from the University of Toronto, Canada, in 1980, 1983 and 1989, respectively. In 1988 he joined the University of Toronto where he is currently a full professor. Dr. Johns has ongoing research programs in analog integrated circuits with particular emphasis on digital communications, oversampling, signal processing, PLLs, ADCs, DACs, and adaptive filtering. His research work has resulted in more than 40 publications as well as the 1999 IEEE Darlington Award. Coauthor of the *Analog Integrated Circuit Design* (Wiley, 1997) textbook, Dr. Johns has given numerous industrial Short Courses. In addition to his academic experience, he has four years of semiconductor industrial experience during 1980, 1983–85, and 1995, and is cofounder of Snowbush, a microelectronics company. He served as an associate editor for *IEEE Transactions on Circuits and Systems* Part II from 1993 to 1995 and for Part I from 1995 to 1997. Dr. Johns is an IEEE Fellow and is already serving on the SSCS AdCom.

Terri S. Fiez received her BS and MS in electrical engineering in 1984 and 1985, respectively, from the University of Idaho, Moscow. In 1990, she received a PhD in electrical and computer engineering from Oregon State University, Corvallis. From 1985 to 1987 and in 1988 she worked at Hewlett-Packard Corporation in Boise and Corvallis, respectively. In 1990 Dr. Fiez joined Washington State University as an assistant professor where she became an associate professor in 1996. In the fall of 1999 Professor Fiez joined the Department of Electrical and Computer Engineering at Oregon State University as a professor and department head.

She became Director of the School of Electrical Engineering and Computer Science in 2003. She has been involved in a variety of IEEE activities including serving on the committees for the IEEE International Solid-State Circuits Conference, IEEE Custom Integrated Circuits Conference, ISCAS, and as a guest editor of the *Journal of Solid-State Circuits*. Dr. Fiez previously was awarded the NSF Young Investigator Award and the Solid-State Circuit Predoctoral Fellowship. Her research interests are in the design of high-performance analog signal-processing building blocks, simulation and modeling of substrate coupling effects in mixed-signal ICs, and innovative engineering education approaches.

Takayasu Sakurai (S'77–M'78–SM'01–F'03) received his PhD in electrical engineering from the University of Tokyo in 1981. In 1981 he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and SOC solutions. He has worked extensively on interconnect delay and capacitance modeling known as the Sakurai model and the alpha power-law MOS model. From 1988 through 1990, he was a visiting researcher at the University of California, Berkeley, where he conducted research in the field of VLSI CAD. Since 1996, he has been a professor at the University of Tokyo, working on low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic ICs and large-area electronics. He has published more than 350 technical publications including 70 invited papers and several books, and has filed more than 100 patents. He served as a conference chair for the Symposium on VLSI Circuits and ICICDT, as a vice chair for ASPDAC and as a program committee member for ISSCC, CICC, DAC, ICCAD, FPGA workshop, ISLPED, TAU and other international conferences. He was a Plenary Speaker for the 2003 ISSCC. He is also an IEEE Fellow, an elected AdCom member of the IEEE Solid-State Circuits Society and an IEEE CAS Distinguished Lecturer.

Mehmet Soyuer received a PhD in electrical engineering from the University of California, Berkeley, in 1988, subsequently joining IBM at the Thomas J. Watson Research Center as a research staff member. His work has involved high-frequency mixed-signal integrated circuit designs, in particular, monolithic phase-locked-loop designs for clock and data recovery, clock multiplication and frequency synthesis using silicon and SiGe technologies. He managed the Mixed-Signal Communications Integrated-Circuit Design group from 1997 to 2000, and since then has been the senior manager of the Communication Circuits and Systems Department at the Thomas J. Watson Research Center, Yorktown Heights, New York.

Dr. Soyuer has authored numerous papers in the areas of analog, mixed-signal, RF, microwave and nonlinear electronic circuit design, and he is an inventor and co-inventor of eight U.S. patents. Since 1997 he has been a technical program committee member of the International Solid-State Circuits Conference (ISSCC). He was an associate editor of the *IEEE Journal of Solid-State Circuits* from 1998 through 2000, and was one of the guest editors for the December 2003 special ISSCC issue. Dr. Soyuer also chaired the Analog, MEMS and Mixed-Signal Electronics Committee of the International Symposium on Low-Power Electronics and Design (ISLPED) in 2001. He is a Senior Member of the IEEE.

Santa Clara Valley Chapter Is Outstanding

The Santa Clara Valley Chapter, the first SSCS chapter, will receive the Outstanding Chapter Award next February at the ISSCC. Jan Van der Spiegel, the SSCS Chapters Coordinator, noted that the SCV Chapter had been "consistently active" since its inception in 1997 with an "impressive list of monthly speakers." The chapter has organized Short Courses and has reached out to local members and students, as reported in the *SSC Newsletter*, July 2004.

The SCV Chapter is the largest SSCS chapter, with 1600 members. In a survey conducted last year, the chapter found it has at least 77 senior IEEE members, and 24 IEEE Life Members. Twenty-three IEEE Fellows belong to the chapter, six of whom are IEEE Life Fellows; there are many prestigious members of the Solid-State Circuits Society in Santa Clara Valley.

Congratulations on a job well done!

Congratulations New Senior Members

Jean-Luc Autran
Eric N. Cartagena
Ramon G. Carvajal
Henry Chang
Ward J. Helms
Vikram B. Krishnamurthy
Tad A, Kwasniewski
Stefan W. Lachowicz
Yuyun Liao
Pradeep Maitra
Dragon Maksimovic
Glenn H. Martin
Masayuki Miyamoto
Arthur S. Morris
Nawej Mwez
Anil Saha
Douglas W. Stout
Dennis M. Sylvester
Marek Syrzycki
Brian K. Swann
Graham E. Town
Chua-Chin Wang
Tin Tin Wee
Stephen T. Williams
Feng Ying
Hoi-Jun Yoo
Benyong Zhang

Listen to Gordon Moore Talk about Moore's Law

The 40th anniversary of Moore's Law is approaching in 2005. Penned in 1965 in *Electronics* magazine, Moore's initial prediction that the number of transistors on an integrated circuit would double annually has been referenced and discussed often in the industry and in the financial press. It was Carver Mead at Cal Tech who called it a law, as if it were a fundamental principal of science or economics. And the behavior of the industry has progressed accordingly. Often IC firms used it to set design goals in their general drive for process and product improvement.

Now the Solid-State Circuits Society makes available online Gordon Moore's Plenary Session presentation on his exponential descriptor of the IC industry. In February 2003 Gordon Moore spoke at the 50th anniversary of the International Solid-State Circuits Conference (ISSCC). The online presentation includes a sound track and the color overheads of graphs and devices over the years.

Download Specifications (requires Microsoft Office Animation Runtime):

- Sample of four slides, 7 minutes runtime, 5M download size
- The complete presentation, 35 minutes runtime, 40M download size

The Web site, *sscs.org/History/MooresLaw.htm*, provides a sample introductory download to test on your system.

The Web site also provides the transcript of the full soundtrack and links to Moore's article and visuals as originally published in the *ISSCC 2003 Digest and Supplement*. Other articles on Moore's Law in IEEE publications are featured on the site. Readers are encouraged to suggest other papers on the future of IC growth and let us know why they think their suggested article should be referenced on the site. Write to a.oneill@ieee.org.

Excerpts from Moore's Presentation

The number of transistors shipped per year has grown $8\frac{1}{2}$ orders of magnitude over the last 35 years. Three hundred million-fold, maintaining an average growth of about 80% per year, now that's a growth industry! Truly phenomenal growth.

To illustrate this number—you're getting up near 10^{18}—I've used raindrops falling on California. Neal Wilson, the Harvard biology expert on ants, estimated that the number of ants in the world is 10^{16} to 10^{17}. So for years I used that. Now each ant has to carry 10^{100} transistors if it's going to take care of its load!

Anne O'Neill
SSCS Executive Director
a.oneill@ieee.org

Call for Fellow Nominations

Nominations are being accepted for the 2006 class of IEEE Fellows. For the second year, nominations, references and endorsements may be submitted electronically. The deadline, 1 March 2005, is two weeks earlier this year.

At its June 2003 meeting, the IEEE Board of Directors approved changes to the process for nominating and electing IEEE members to Fellow grade. The change established a new nomination category for individual contributions, with the goal of increasing nominations for members in industry and encouraging nominations of application engineers or engineering practitioners who have made contributions of unusual distinction to the profession.

The board also established a Fellow Nomination Resource Center to help nominators locate the required number of references to support a nomination.

To nominate an IEEE senior member or to learn more about the Fellow program, visit *www.ieee.org/fellows*.

IEEE Virtual Museum Praised by *ScientificAmerican.com*

The IEEE Virtual Museum is among five Web sites chosen by ScientificAmerican.com for its Science & Technology Web Awards 2004 in the Engineering & Technology category.

According to ScientificAmerican.com, the 50 sites chosen overall represent the "best sites from the rest" and are "worthy of high praise." In reference to the IEEE Virtual Museum, ScientificAmerican.com told readers, "Start digging—you'll be just as grateful as the Institute expects you to be!"

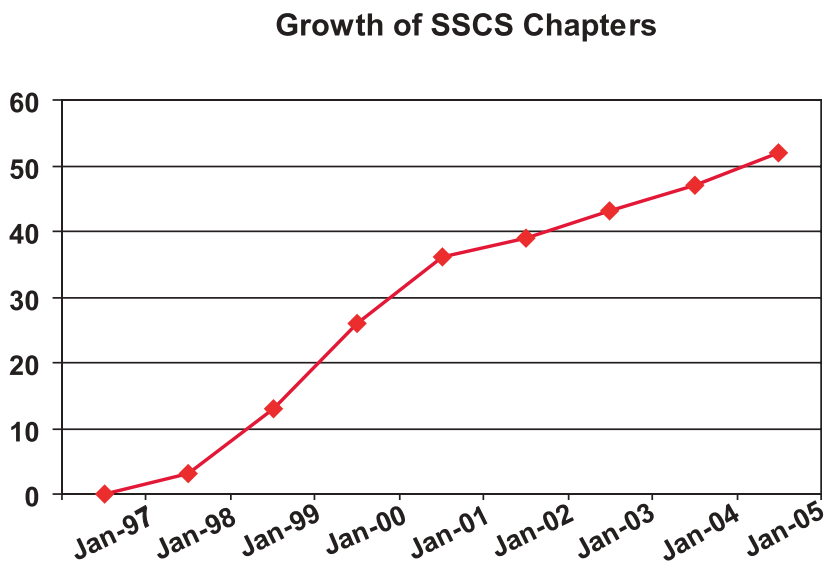
For more information, visit *www.ieee-virtual-museum.org/*.

SSCS Tops 50 Chapters

With the addition of five new chapters that were formed during the last half of 2004, the Solid-State Circuits Society has exceeded its goal of 50 chapters, as was envisioned at its founding in 1997. The prediction of our chapter chair coordinator, Jan Van der Speigel, was realized in July of 2004.

SSCS would like to extend a warm welcome to the five new chapters that helped put us at the top. Two of the new chapters are singularly focused on the SSCS field of interest: the Tucson Chapter, chaired by Joseph Wu, and the Vancouver Chapter, chaired by Resve Saleh. The Central North Carolina Chapter shares the fields of interest of SSCS and Electron Devices (EDS) and is chaired by Tony Ivanov. Two new joint SSCS/Circuits and Systems Society (CAS) chapters are the Southern Alberta Chapter, chaired by Caitlin Davis, and the Canada Atlantic Chapter, chaired by Marc Murphy. (Chapters devoted to the technical interests of more than one society are described as joint.)

More than half of all SSCS chapters are singularly focused on the SSCS technical interests. Thirty percent of SSCS chapters are joint chapters with only one other society technical interest. Nine chapters are joint with only EDS, seven chapters are joint with only CAS, and one joint with SPS. The remaining nine are joint with multiple societies.

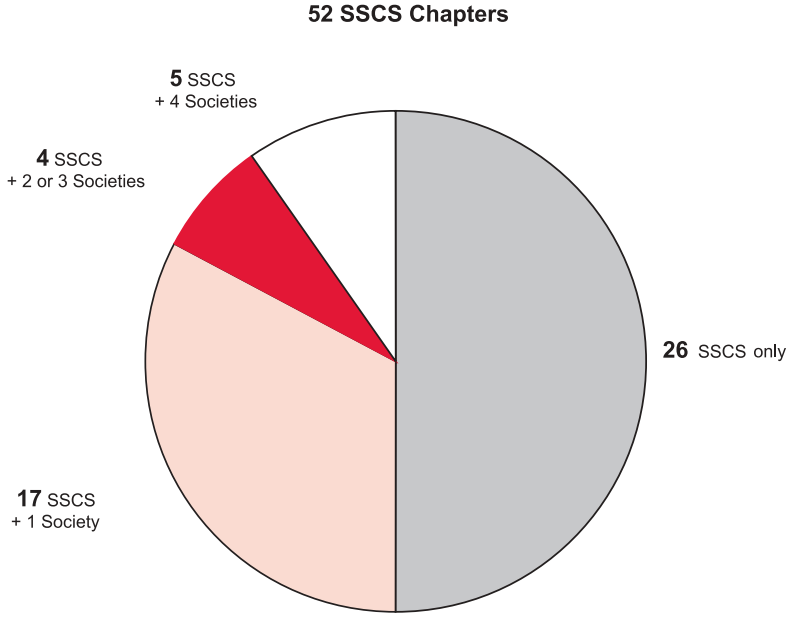


The Society has chapters in nine regions worldwide. There are currently thirteen chapters in regions 1–6 (U.S.), seven in region 7 (Canada), twenty-two in region 8 (Europe and Africa), and ten in region 10 (Asia and Australia). The Society's goal is to continue chapter formation.

Van der Speigel commented on the achieving the goal, "It is very exciting to see the strong interest in SSCS chapters. The healthy growth of the SSCS chapters is a good indicator of the involvement of the members in SSCS related activities worldwide. I would like to take the opportunity to thank all the chapter officers for their efforts in offering educational and professional activities to their members."

To see if there is an SSCS chapter near you, visit our online roster at *sscs.org/Chapters/chptrchairs.htm*. For tips, instructions and petition forms to start a chapter in your city check out this URL: *sscs.org/chapter.htm#startchapter*.

Chapter chairs meet annually over lunch during the February ISSCC in San Francisco to discuss best practices. If you are interested in starting a chapter, contact Jan Van der Speigel at jan@seas.upen.edu.



Chapter News

Denver Chapter

During the past half year, the SSCS Denver Chapter hosted several technical seminars and a social event. In May 2004 Michael Rubin of Agilent Technologies presented "IC design solutions in a foundry environment," an important topic especially given the concentration of fabless design houses in northern Colorado. Due to summer tapeout pressures encountered by the chapter officers, chapter activities resumed in September with a BBQ social at a local clubhouse. The following month, Ken Richardson of LSI Logic presented an informative tutorial on "Measurement, modeling, and simulation of high-speed transmission lines." This was a particularly applicable seminar since many local companies in Fort Collins have active R&D efforts in developing high-speed serial data interfaces.

Our year ended with a seminar on the globalization of engineering and high-tech jobs, a topic that attracted participation from over one hundred people—the largest attendance since the chapter's inception two years ago! Dr. Don Morris, recently retired from Agilent Technologies, gave a thoroughly insightful presentation on the controversial topic. He drew upon classical economic thought and provided powerful historical examples of high technology and international trade dating back many centuries in order to motivate the conclusion that the outsourcing of commoditized engineering activity to lower-cost geographies is merely an inevitable and natural economic evolution driven by the "cold, dead hand of Adam Smith." Alluding to his experiences managing a design lab he created in Singapore, Dr. Morris also explained that the high-tech sector in Singapore was in deep fear of job outsourcing to even lower-cost geographies. The key to surviving through such economic trends is to embrace outsourcing whenever and wherever possible in order to enjoy cost advantages sooner than competitors, but continue to innovate new products, hence creating new activities to replace outsourced ones. On a personal level, this requires continual development of new skills that enable such innovations so as to maintain marketability.

The new Atlantic (Canada) Chapter: Section Chair Ken Mah, Chapter Chair Marc Murphy, and Guest Speaker Farhad Shafai. The Atanatic Chapter, joint SSCS and CAS is online at www.ieee.org/cas_ckts

The 2005 annual elections were also held in November with Dr. Alvin Loke elected as Chapter Chair, Dr. Don McGrath as Vice Chair, Tin Tin Wee as Secretary/Web master, and Bob Barnes as Treasurer.

We look forward to growing participation in upcoming seminars. Please visit our Web site at *ewh.ieee.org/r5/denver/sscs/* for more information (including past presentation slides) about our chapter events.

Alvin Loke
Denver Chapter Vice Chair
alvin.loke@ieee.org

Tin Tin Wee
Denver Chapter Secretary/Web master
tintin.wee@ieee.org

Hans Stork spoke in July to the San Diego Chapter on the Realities of System-on-Chip Integration.

ED/SSC Varna Chapter

The Technical University of Varna, Bulgaria, held a three-week summer school on CAD in electronics, funded primarily by the joint IEEE Solid-State Circuits and Electron Devices Chapter. There were lectures and practical training by faculty from the Technical Universities of both Varna and Sofia. The main topic was analog IC design, simulation, and layout

using Pspice and Cadence software products. Of the sixteen in attendance, half were IEEE members.

In the fall of 2003 the Varna Chapter cosponsored two technical meetings. As a part of the Conference ET2003 (Electronic Engineering 2003) in Sozopol, whose primary sponsor was the TU of Sofia, more than 100 papers were presented in the sessions. As part of the anniversary conference of the Technical University of Gabrovo, there were over 90 papers presented in the sessions on electrical engineering, computer science and engineering, electronics, and communications.

Jordan Kolev
SSCS Bulgaria Chapter Chair
ikolev@ieeel.bg

Kansai Chapter

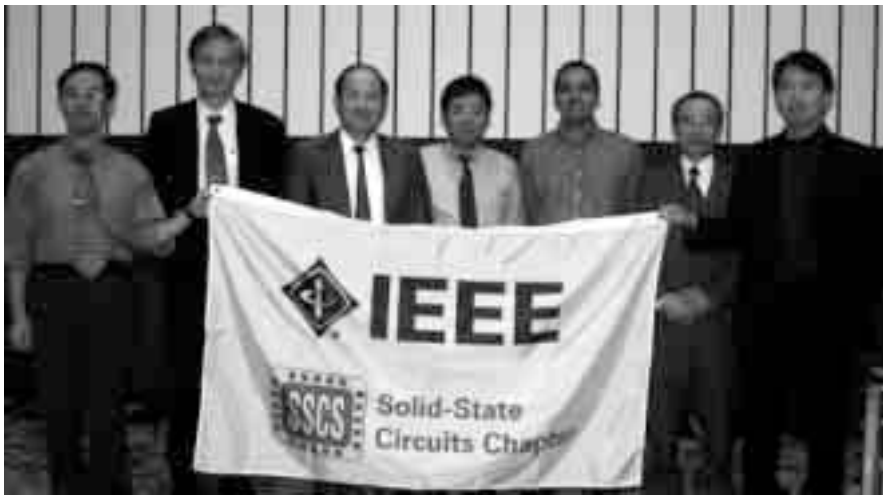
The Kansai Chapter held a technical seminar on 25 October in Kyoto, focusing on interconnects in terms of signal integrity in nanometer-scale designs. Two excellent speakers attracted an audience from across Japan, including 34 professionals and 12 students.

Toshiki Kanamoto from Renesas Technology Corporation provided a tutorial lecture on "Interconnect modeling technology for SoC design," introducing the basics of timing analysis, interconnect modeling and extraction technologies. He also provided insights into the practical consideration of inductive parasitics in SoC design with the latest EDA tools.

Dr. Nishath Verghese from Cadence Design Systems dealt thoroughly with delay calculation for gate models that accurately accounted for long wires, crosstalk, ground bounce, temperature inversion, as well as process variability. The interplay of crosstalk and timing was covered in his presentation, "Accurate crosstalk and timing analysis of nanometer-scale digital ICs."

Both talks were well organized, providing a good reference for experienced designers as well as motivating students towards innovative thesis work in the VLSI design field. Questions from the audience and answers by the lectures were very detailed and helped further understanding of the topics, which characterized the success of the seminar.

Makoto Nagata
Kansai Chapter Secretary
mnagata@ieee.org



Kansai Chapter at 25 October 2004 seminar (left to right) : Junji Ishikawa (Treasurer), Hironori Yamauchi (Chapter Vice Chair), Masao Nakaya (Chapter Chair), Toshiki Kanamoto (Invited lecturer), Nishath Verghese (Invited lecturer), Hidetoshi Onodera (Former Chair of Kansai Chapter) and Makoto Nagata (Secretary).

2003–2004 Membership Report

The SSCS membership dropped 7.8% from May 2003 to May 2004. Other IEEE societies experienced similar attrition (see the table below). The Communications Society enjoyed an increase in membership from February 2004 to May 2004 due to more than 10,000 new student members.

Membership Drop from 2003

Societies	Feb 2004	March 2004	May 2004
CAS	-17.4% (11,075)	-17.2% (11,535)	-17.6% (11,924)
ED	-6.0% (10,682)	-6.7% (10,962)	-6.8% (11,188)
LEO	-3.7% (7,079)	-4.6% (7,376)	-5.4% (7,695)
COM	-9.3% (38,932)	-0.3% (40,310)	5.4% (45,360)
SP	-2.3% (14,402)	-2.5% (14,648)	-3.9% (15,053)
SSC	-7.1% (11,319)	-7.1% (11,682)	-7.8% (11,966)

IEEE

In July 2004 the IEEE performed an All-Society Research Project (ASRP). The goals of ASRP were threefold:

- Gather data from individuals who maintained their IEEE membership but dropped their society membership in one or more IEEE societies.
- Identify the reasons for the declining membership.
- Identify potential improvements in products and services.

For SSCS, 1077 current IEEE members who dropped their SSCS membership were invited to participate, and a total of 281 former Society members completed surveys for a 26% response rate. The demography of the "population" who dropped SSCS membership is summarized in the following table.

Member Grade

Member Grade	# of Respondents (in sample)	Sample %	Population %
Member	170	61%	66%
Student	76	27%	22%
Senior Member	20	7%	7%
Associate	12	4%	4%
Fellow	3	1%	2%
Life (All grades)	0	0%	0%
Total	**281**	**100%**	**100%**

IEEE

Of the "population," 52% were with private industry, 18% were full-time students, and another 18% were with educational institutions. The high percentage of dropped memberships in private companies reflected the spending cuts within the semiconductor industry in the past few years.

When asked to give their reasons for dropping SSCS membership, four major factors were quoted to have influenced their decisions:

- My employer/university has access to IEEE publications and I feel I no longer need my personal IEEE SSCS membership (31%)
- I do not have time to read IEEE SSCS publications (30%)
- My career/position has changed and IEEE SSCS is no longer relevant (28%)
- IEEE SSCS membership dues are too expensive (23%)

When asked if they would choose to rejoin SSCS in the next year, 52% said unlikely, 31% undecided, and only 17% said likely. Since 56% of them also quoted that the reason they joined SSCS in the first place was to obtain SSCS publications, the availability of IEEE publications online would have a continual effect on our membership enrollment.

When asked why they were dissatisfied with the SSCS membership specifically, the high cost of membership fees and the *JSSC* publication charges were ranked distinctly the top issues. Changed job functions and narrow focus of the Society publications on analog design were two other major factors.

When asked what the SSCS could do to regain their patronage, over 50% wanted a reduced membership fee and access to online publications at no extra cost. A more interesting suggestion was to create an *SSCS Magazine*, similar to the *Communications Magazine*, which can serve the circuit-design professionals at large. For example, the articles in the magazine can be devoted to a broader coverage of various circuit design disciplines, explanations of current and breaking technologies, and tutorials on design techniques, rather than the detailed research papers, as currently published in *JSSC*. Providing more local activities for networking and job-related opportunities and helping young engineers realize their career goals were also mentioned as lacking in our Society services.

Finally, a survey on IEEE publications indicated that *JSSC* was voted the most "useful" among all IEEE publications (59.8% "extremely useful"), and that ISSCC was also voted the most useful among all IEEE-sponsored conference proceedings. In general, the majority of our members feel well served due to our high-quality publications and conferences. However, we may have a challenging task ahead to reach out to more engineers, especially the younger ones. We will need to provide a broader base of knowledge and services to accommodate the shift in focuses of the semiconductor industry over time.

Teresa Meng
SSCS AdCom
Membership Chair
thm@stanford.edu

Hirohisa Kawamoto Named Steering Committee Chair of IEEE/OSA *Journal of Display Technology*

Hirohisa Kawamoto is the chair of the first steering committee organized to launch the new IEEE/OSA *Journal of Display Technology* (JDT) in 2005. Kawamoto, an IEEE Fellow, is a visiting professor at Nara Institute of Science and Technology, Takayama, Nara, Japan. He received his BS degree in electronics from Kyoto University, Japan, in 1961 and his MS and PhD degrees in electrical engineering and computer sciences from the University of California, Berkeley, in 1966 and 1970, respectively.

From 1961 to 1968 he was with the Matsushita Electronic Corporation, Osaka, Japan. In 1970 he taught as an acting assistant professor at the Department of Electrical Engineering and Computer Sciences of the University of California, Berkeley. From 1970 to 1980 he worked for the RCA David Sarnoff Research Center, Princeton, New Jersey. In 1980 he founded the Sony Consumer Electronics Laboratories in Paramus, New Jersey, where he served as general manger until 1985. During the same time he founded the Princeton Community Japanese Language School, Princeton, New Jersey, and served as the chair of its Board of Trustees until 1985.

From 1985 to 2001 he was with the Sharp Corporation, Japan, where he participated in the founding of Sharp Laboratories of Europe at Oxford, U.K., and Sharp Laboratories of America at Camus, Washington. His last assignment at Sharp was as vice president and division general manager of the Technical Information Center.

Since July 2001, he has been a senior business advisor with Silicon Image Inc., Sunnyvale, California, stationed in Nara Gakuen-Mae, Japan. From 1994 to 2000 he acted as a delegate from Japan to the Committee of Action of International Electro-Technical Commission, Geneva, Switzerland.

Dr. Kawamoto was elevated to IEEE Fellow in 1992 for contributions to materials, device, and systems technologies for the use in video systems. Dr. Kawamoto has also received the IEEE Centennial Medal and Third Millennium Medal.

Call for Papers and Subscribers

The *JDT* will cover display systems and engineering, materials and components, optical design, lighting technologies, display drivers and interfaces, display packaging, manufacturing technology, reliability and testing, and applications. Manuscripts can be submitted electronically for peer review thorough IEEE's Manuscript Central *http://www.i-leos.org/*. Sponsored by seven IEEE societies including SSCS, the peer review process for *JDT* is managed through the staff of the Laser and Electro-optics Society (LEOS). New authors should create an account. Authors who have previously submitted manuscripts to LEOS publications could simply select the *IEEE/OSA Journal of Display Technology* and log on. For questions, contact Linda Matarazzo, Manager, IEEE LEOS Editorial Office, l.matarazzo@ieee.org (phone +1 732 562 3910; fax +1 732 981 1138).

The inaugural issue of the *JDT* is scheduled for September 2005. The mid-year introduction in 2005 will be followed by quarterly publication in 2006. The member prices for the introductory year will be $13 for online, $14 for print, and $17 for both in 2005, reflecting just two issues printed in the launch year. In 2006, when four issues will be printed, subscription rates will be adjusted. Subscriptions are available at any time by choosing to "Add Services" to your membership record: *http://services1.ieee.org/membersvc/addservices/intro.htm*.

Books of Interest to SSCS

This selection of technical books covers topics that may be of interest to our readers. The descriptions are provided by the publishers.

Electronic Physical Design
by Barry M. Lunt, PhD, Brigham Young University, published by Prentice Hall, 2004, $91.00, ISBN: 0-13-094387-8.

Electronic Physical Design is a useful reference for both the theory and practice of electronic physical design for courses in areas such as electronic manufacturing processes, electronic physical design, circuit board design, and electronic prototyping. This text addresses the choices to be made at the IC level, the IC package level, and the circuit board level. It then discusses the choices among the many types of resistors, capacitors, connectors, and transistor packages. Finally, this text addresses the concepts involved in building high-quality products, including robust design, heat vibration, shock, dust, and humidity.

Fundamentals of Electric Circuits (Third Printing) with CD-ROM (Second Edition)
by Charles Alexander, Cleveland State University, and Matthew Sadiku, Prairie View A&M University, published by McGraw-Hill, 2004, price to be announced, ISBN: 0-07-304835-6.

Fundamentals of Electric Circuits

is intended for use in the introductory circuit analysis or circuit theory courses taught in electrical engineering or electrical engineering technology departments. The main objective of this book is to present circuit analysis in a clear, easy-to-understand manner, with many practical applications. Each chapter opens with either historical sketches or career information on a subdiscipline of electrical engineering. This is followed by an introduction that includes chapter objectives. Each chapter closes with a summary of the key points and formulas.

The authors present principles in an appealing and lucid step-by-step manner, carefully explaining each step. Important formulas are highlighted to help students sort out what is essential and what is not. Many pedagogical aids reinforce the concepts learned in the text so that students become comfortable with the various methods of analysis presented in the text.

Formal Verification
by Douglas Perry and Harry Foster, to be published by McGraw-Hill Professional, 2005, $89.95, ISBN: 0-07-144372-X.

Formal verification is a powerful new digital design method. In this cutting-edge tutorial, two of the field's best-known authors team up to show designers how to efficiently apply formal verification, along with hardware description languages like Verilog and VHDL, to more efficiently solve real-world design problems.

An Introduction to Radio-Frequency Engineering
by Christopher Coleman, published by Cambridge University Press, May 2004, £40.00, ISBN 0-52-183481-3.

This book provides an excellent introduction to radio-frequency engineering, using a straightforward and easily understood approach combined with numerous examples, illustrations, and homework problems. The author focuses on minimizing the mathematics needed to grasp the subject while providing a solid theoretical foundation for the student. Emphasis is also placed on the practical aspects of radio engineering. The book provides a broad coverage of RF systems, circuit design, antennas, propagation, and digital techniques. Written for upper-level undergraduate courses, it also provides an excellent introduction to the subject for graduate students, researchers and practicing engineers.

Introduction to Semiconductor Devices for Computing and Telecommunications Applications
by Kevin Brennan, published by Cambridge University Press, December 2004, £40.00, ISBN: 0-52-183150-4.

From semiconductor fundamentals to state-of-the-art semiconductor devices used in the telecommunications and computing industries, this book provides a solid grounding in the most important devices used in the hottest areas of electronic engineering today. The book includes coverage of future approaches to computing hardware and RF power amplifiers, and explains how emerging trends and system demands of computing and telecommunications systems influence the choice, design, and operation of semiconductor devices. The book begins with a discussion of the fundamental properties of semiconductors. Next, state-of-the-art field-effect devices are described, including MODFETs and MOSFETs. Short-channel effects and the challenges faced by continuing miniaturization are addressed. The rest of the book discusses the structure, behavior, and operating requirements of semiconductor devices used in lightwave and wireless telecommunications systems. This is an excellent senior/graduate text, and a valuable reference for engineers and researchers in the field.

Low-Voltage, Low-Power VLSI Subsystems
by Kiat-Seng Yeo and Kaushik Roy, to be published by McGraw-Hill Professional, 2005, $130.00, ISBN: 0-07-143786-X.

There is no better way to learn the latest techniques in VLSI design than *Low-Voltage, Low-Power VLSI*. An invaluable reference and practical guide to the latest in optimized VLSI subsystem design, written by leaders in cutting-edge chip design, this focused tutorial offers immediate access to state-of-the-art, proven techniques in CMOS, BiCMOS, and other in-demand applications. To designers already hard at work in the $200-billion-per-year-and-growing electronics marketplace, and to students who want to join this fast-track industry, Kiat-Seng Yeo and Kaushik Roy offer

- New approaches to the challenges of silicon-level design for low-power circuitry pacing electronics
- Low-power solutions for SRAMs, DRAMs and signal processors
- Expert performance comparisons and contrasts of low-power options
- Reduced-complexity design solutions
- Optimization and implementation techniques indispensable in modern VLSI subsystem design
- Useful charts, illustrations, and applied algorithms
- Clear presentations of complex topics
- Real-life examples clarifying key concepts

Mobile Wireless Communications
by Mischa Schwartz, published by Cambridge University Press, December 2004, £40.00, ISBN: 0-52-184347-2.

Wireless communication has become a ubiquitous part of modern life, from global cellular telephone systems to local and even personal-area networks. This book provides a tutorial introduction to digital mobile wireless networks, illustrating theoretical underpinnings with a wide range of real-world examples. The book begins with a review of propagation phenomena, and goes on to examine channel allocation, modulation techniques, multiple access schemes, and coding techniques. GSM and IS-95 systems are reviewed and 2.5G and 3G packet-

switched systems are discussed in detail. Performance analysis and accessing and scheduling techniques are covered, and the book closes with a chapter on wireless LANs and personal-area networks. Many worked examples and homework exercises are provided and a solutions manual is available for instructors. The book is an ideal text for electrical engineering and computer science students taking courses in wireless communications. It also is a valuable reference for practicing engineers.

PSpice for Basic Circuit Analysis (First Edition)
by Joseph G. Tront, Virginia Polytech Institute & State University, published by McGraw-Hill, 2004, price to be announced, ISBN: 0-07-298509-7.

PSpice for Basic Circuit Analysis introduces readers to the fundamental uses of PSpice in support of basic circuit analysis. This book is designed so that the reader may advance rapidly to solving a variety of circuit analyses. Although the fundamental capabilities of PSpice are covered in this book, the principles can easily extend to analyze the complex electrical and electronic networks used in modern integrated circuit design today.

RapidIO—The Embedded System Interconnect
by Sam Fuller, published by John Wiley & Sons, January 2005, $135.00, ISBN: 0-470-09291-2.

RapidIO was developed specifically to achieve high-performance, low-cost, reliable and scalable system connectivity in embedded, networking and communications devices. Written by one of the founders of the RapidIO Trade Association, this is the first comprehensive reference on this interconnect technology. It covers logical layer protocols, network, link and physical layer technologies, packet and symbol formats, register file definitions, and system software application programming interfaces. The book:

- Discusses the usage of RapidIO in embedded systems such as enterprise storage and wireless infrastructure
- Illustrates newly defined technologies such as the RapidFabric dataplane extensions
- Describes case studies of RapidIO usage in real system architectures
- Evaluates the programming models associated with RapidIO
- Reviews related mechanical standards such as the VME Switched Serial Extensions and the PICMG Advanced Telecommunications Architecture (ATCA) standards

RF Power for Industrial Applications
by Louis E. Frenzel, Jr., published by Prentice Hall, 2004, $95, ISBN: 0-13-096577-4.

Written for two- to four-semester-hour courses in RF power in the electronics/computer technology departments, *RF Power for Industrial Applications* also can be used for industry courses in RF power. This text, the only one of its kind on the market, focuses on RF power for use in industrial applications, where semiconductor manufacturing equipment generates a plasma for processing wafers. The emphasis is on equipment and circuits related to RF power in manufacturing equipment tools such as etchers and chemical vapor deposition, among others. This is a useful book that provides a base upon which a student can pursue more equipment-specific knowledge.

Silicon Germanium: Technology, Modeling, and Design
by Raminderpal Singh, Modest M. Oprysko, and David Harame, published by Wiley-IEEE Press, 2004, $99.95, ISBN: 0-471-44653-X.

Written for RF/analog and mixed-signal designers, CAD designers, semiconductor students, and foundry process engineers worldwide, *Silicon Germanium* provides detailed insight into the modeling and design automation requirements for leading-edge RF/analog and mixed-signal products, and illustrates in-depth applications that can be implemented using IBM's advanced SiGe process technologies and design kits. The book:

- Discusses IBM's design automation and signal integrity knowledge and implementation methodologies
- Highlights details of highly integrated SiGe BiCMOS System-On-a-Chip (SOC) design

Tech Mining: Exploiting New Technologies for Competitive Advantage
by Alan L. Porter, Georgia Institute of Technology, Atlanta, and Scott W. Cunningham, published by John Wiley & Sons, November 2004, $69.95, ISBN: 0-471-47567-X.

Tech Mining incorporates the premise that the information, the tools to exploit it, and the need for resulting knowledge is available and provides the comprehension needed to enable technology managers to utilize new capabilities. By using the lessons presented in the book, managers can identify and access the most valuable technology information resources; search, retrieve, and clean the information on topics of interest; and lower the costs and enhance the benefits of competitive technological intelligence operations.

WCDMA for UMTS: Radio Access for Third-Generation Mobile Communications (Third Edition)
by Harri Holma and Antti Toskala, both of Nokia, Finland, published by John Wiley & Sons, September 2004, $105.00, ISBN 0-470-87096-6.

Regarded as "the book" on the air interface of 3G cellular systems, *WCDMA for UMTS* has been fully revised and updated. Now detailing the key features of 3GPP Release 6, this book remains the leading resource in this constantly progressing area. By providing a deep understanding of the WCDMA air interface, the practical approach will continue to appeal to operators, network and terminal manufacturers, service providers, university students, and frequency regulators.

SSCS EVENTS CALENDAR

Also posted on *www.sscs.org/meetings*

SSCS SPONSORED MEETINGS

2005 ISSCC International Solid-State Circuits Conference
www.isscc.org
6–10 February 2005
San Francisco Marriott Hotel, San Francisco, CA, USA
Paper deadline: passed
Contact: Courtesy Associates, ISSCC@courtesyassoc.com

2005 Symposium on VLSI Circuits
www.vlsisymposium.org
16–18 June 2005
Kyoto, Japan
Paper deadline: 7 January 2005
Contact: Phyllis Mahoney, vlsi@vlsisymposium.org or Business Center for Academic Societies, Japan, vlsisymp@bcasj.or.jp

2005 CICC Custom Integrated Circuits Conference
www.ieee-cicc.org
18–21 October 2005
San Jose, CA, USA
Paper deadline: awaiting
Contact: Ms. Melissa Widerkehr, cicc@his.com

2005 A-SSCC Asia Solid-State Circuits Conference (the first meeting)
a-sscc.org/
1–3 November 2005
Taiwan
Paper deadline: 31 May 2005
Contact: org@a-sscc.ee.ntu.edu.tw

SSCS PROVIDES TECHNICAL CO-SPONSORSHIP

VLSI-TSA International Symposium on VLSI Technology
vlsitsa.itri.org.tw
25–27 April 2005
Hsinchu, Taiwan
Paper deadline: passed

2005 International Conference on VLSI Design
www.isical.ac.in/~vlsi2005
3–7 June 2005
Taj Bengal, Kolkata, India
Paper deadline: passed

2005 Radio Frequency Integrated Circuits Symposium
www.rfic2005.org
12–14 June 2005
Long Beach, CA, USA
Paper deadline: 3 January 2005

2005 Design Automation Conference
www.dac.com
13–17 June 2005
Anaheim, CA, USA
Paper deadline: passed

2005 Symposium on VLSI Technology
www.vlsisymposium.org
14–16 June 2005
Kyoto, Japan
Paper deadline: 7 January 2005

2005 European Solid-State Circuits Conference
www.esscirc2005.org/
12–16 September 2005
Grenoble, France
Paper deadline: 9 April 2005

2005 International Conference on Computer-Aided Design
www.iccad.org
6–10 November 2005
San Jose, CA, USA
Paper deadline: 20 April 2005

IEEE SOLID-STATE CIRCUITS SOCIETY NEWSLETTER (ISSN 1098-4232) is published quarterly by the Solid-State Circuits Society of The Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. $1 per member per year (included in society fee) for each member of the Solid-State Circuits Society. This newsletter is printed in the U.S.A. Periodicals postage paid at New York, NY and at additional mailing offices. **Postmaster:** Send address changes to IEEE Solid-State Circuits Society Newsletter, IEEE, 445 Hoes Lane, Piscataway, NJ 08854.

To maintain all your IEEE and SSCS subscriptions, email address corrections to *address-change@ieee.org*
To make sure you receive an email alert, keep your email address current at *sscs.org/e-news*

445 Hoes Lane
Piscataway, NJ 08854