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The 2007 International Solid State Circuits Conference, slated to convene in San Francisco Feb. 11 through 15, features a theme of multidimensionality. Declaring that in an age of nanoscale devices and macro-scale variations, only comprehensive teamwork between process engineers, circuit designers, chip architects, and systems designers can make major advances, the premier conference on IC design will illustrate that point with seven full-day design forums, four short courses, 10 tutorials, 182 full-length papers, plus short papers and evening sessions.

In the process, the technical papers also illustrate another point: The days in which scaling could be counted on to deliver greater performance and better density with little technical innovation are over. Papers in processor design, analog design, and packaging are beginning to show a profound rethinking of basic assumptions about the roles of architecture and system design in the four dimensions of chip engineering.

In the world of CPUs, for instance, for the first time ever all of the papers in the microprocessor section describe multicore chips. These range from dual-core designs (the IBM Power6, PA Semi PWRficient, and Intel Merom) to the extreme outlier of the group: a 65-nm design from Intel that combines 80 tiles, each with a floating-point core and a packet-switching router, into a 4-GHz, 1.0-TFLOP on-chip processing network.

Along with the large numbers of transistors and multi-gigahertz speeds comes the need for dynamic power management. Papers will describe increasingly comprehensive networks of sensors deployed across chips to monitor current, temperature, voltage noise, and other operating parameters, as well as increasingly sophisticated means of dynamic threshold, supply-voltage, and frequency scaling to keep the chips within their operating envelopes. At the extreme end of this effort, a paper from National Chung-Cheng University in Taiwan will described a 32-bit RISC core implemented in ultralow-voltage CMOS circuitry that operates on as little as 230 mV. Another paper will describe a possible power source for such circuits—a device that scavenges both RF and thermal energy from its environment and converts the energy for storage in a nearby battery.

But as one of the plenary session speakers, Analog Devices Fellow Lewis Counts, will observe, the end-point of dimension and voltage scaling lies in an analog world. On the low-voltage front, one paper will describe a 2.5-GHz, 90-nm fractional-N synthesizer operating at 650 mV. Papers will describe voltage regulators intended to be embedded in SOCs, including a buck converter that recycles charge from a 3-GHz system clock to improve its efficiency.

Indicating that 90-nm technology is no barrier

to precision analog, no fewer than eight papers will describe data converters in this geometry. Meanwhile, CMOS frequency limits are being crushed by papers describing 40- to 90-GHz CMOS circuits and a set of millimeter-wave components operating at up to 104 GHz in 90-nm CMOS.

Along with architecture and circuit design, packaging is coming to the fore at the conference, with a number of papers devoted to three-dimensional packaging techniques. Perhaps the most novel describe efficient capacitive- and inductive-coupling techniques for passing very-high-frequency signals between dice in 3D configurations.

Finally, a growing trend at the conference is the emergence of medical applications for IC technology. A session on biomedical devices will describe a seemingly science-fiction world of dense implantable sensors that interact with nerve cells, a chip designed to stimulate retinas for visual prosthesis, and an adaptive-hearing-aid chip. Other sessions will explore body-area networks and wireless sensor interfaces for grouping such devices into monitoring and prosthesis systems for human bodies.

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