[Technology Report]

ADCs At ISSCC

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ED Online ID #11839
January 12, 2006

For the latest and greatest, take a look at what's coming up at this year's International Solid-State Circuits Conference (ISSCC), scheduled for Feb. 4-8 in San Francisco.

As noted above, the delta-sigma architecture is enjoying a rennaisance, at remarkably high input signal frequencies. Xignal will disclose the details of its continuous-time, delta-sigma converter in a paper titled ?A 14b 20 mW 640MHz CMOS Continuous-Time ΣΔ ADC with 20-MHz Signal Bandwidth and ENOB of 12.?

Next, there's ?A 375-mW Quadrature Bandpass ΔΣ ADC with 90-dB DR and 8.5-MHz BW at 44 MHz.? Written by a group of ADI authors, it explains ?the new and increasing number of digital standards, provid[ing] the impetus for developing a universal receiver [that] relies on digital signal processing for the channelization and decoding operations.? Their work led to an ADC that accepts a quadrature 44-MHz IF input. It boasts an 83-dB dynamic range spec and a full-scale (automatic gain control) range of 12 dB.

Authors from Delft University of Technology and Philips will offer ?An 118dB Dynamic Range Continuous-Time IF-to-Baseband SD Modulator for AM/FM/IBOC Radio Receiver.? It describes another multistandard CMOS continuous-time (CT) sigma-delta modulator with integrated mixer. It eliminates the variable gain amplifier and external AM channel filter in AM/FM radios. The modulator digitizes a radio signal at a 10.7-MHz IF with a 118-dB dynamic range for AM and a 98-dB dynamic range for FM, with a 90-dB in-band on-channel (IBOC) spurious-free dynamic range.

In a similar vein, there's ?An 80/100Msps, 76.3/70.1dB SNDR ΔΣ ADC for Digital TV Receivers.? Prepared by authors from Sharp, it illustrates a wideband delta-sigma ADC with a double-sampling and operational-transconductance amplifier optimization that achieves a 76.3/70.1-dB peak signal-to-noise plus distortion ratio (SNDR) over a 3.2/4-MHz bandwidth while consuming 23.8/34.4 mW from a 1.8-V supply.

The renewed popularity of the delta-sigma architecture and its application at radio frequencies is due in part to the availability of fine-geometry CMOS process technologies. The low operating voltages associated with advanced processes, however, present dynamic range and noise issues.

This is acknowledged in ?A 0.5V 74dB SNDR 25kHz CT ΣΔ Modulator with Return-to-Open DAC.? Its authors from the Chinese University of Hong Kong and Columbia University in New York note that ?the continuous reduction of minimum feature sizes in modern CMOS technologies into

the nano-scale requires a proportional reduction of the supply voltage to well below one volt to maintain reliability.

?At the same time, the threshold voltage of the devices is not scaled in the same proportion to limit leakage currents for digital circuits. The combination of low supply voltages and high device thresholds poses very challenging constraints on analog circuit design.?

The authors then describe how they developed a 0.5-V continuous-time, third-order, delta-sigma modulator in CMOS that doesn't use any special low-voltage devices nor any internal voltage boosting.

ISSCC has more on the plunge into fine-geometry CMOS ADCs that don't use the delta-sigma architecture. For display and image processing, the need to balance speed, accuracy, and power led to the now familiar figure of merit (FoM) for ADCs:

$$FoM = power/(2^{ENOB} * F_{s,nyq})$$

where $F_{s,nyq}$ is the Nyquist frequency.

And, Philips offers ?A 90nm CMOS 1.2V 10 b Power and Speed Programmable Pipelined ADC with 0.5 pJ/Conversion-Step.? Previously, the literature reported 1-pJ FoMs for 10-bit ADCs optimized at a sampling frquency (F_s) of 1, while ADCs with programmable speed and power show a 1.5-pJ FoM. Philips' 2006 ISSCC paper presents a new ADC with programmable speed and power showing a 0.5-pJ FoM over a large range of sample frequencies. Implemented in 90-nm digital CMOS technology, the chip runs on 1.2 V.