SYLLABUS ELEN E4321: VLSI Circuits Fall 2001 (01)

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Office Hours:	TF2-4 (tentative) 1212 Mudd (no phone yet)
Class Time:	MW11-12:15
Class Location:	1024 Mudd
Class Homepage:	http://www.cisl.columbia.edu/courses.html -> E4321
Credits / Type:	3 / Lecture
Prerequisites:	Recommended ELEN E3301, E3910, & E3106
Required Text:	Digital Integrated Circuits: A Design Perspective, by Jan M. Rabaey, Prentice Hall, Inc.
Homework(s):	Generally due each Wednesday
Project(s):	Mini Design Project in last few weeks
Midterm Exam(s):	One exam on 10/24 (one page of notes)
Final Exam:	During final exam period (two pages of notes)
Grading:	20% Problem Sets, 20% Midterm, 20% Mini-project, 40% Final
Software:	Remote Access to Columbia CAD Tools - Details TBA
Homework Submit:	Fax / Postmark / Email / Hand in to TA by due date at latest

COURSE OUTLINE (tentative)

Date	Class	Topic	Out	In
9/5	1	VLSI Overview & History	PS 1	
9/10	2	Overview - Digital CMOS Technology		
9/12	3	Overview - Digital CMOS Circuits	PS 2	PS 1
9/17	4	Review of Semiconductor Dev Models		
9/19	5	MOS Transistors I	PS 3	PS 2
9/24	6	MOS Transistors II		
9/26	7	Interconnect Modeling I	PS 4	PS 3
10/1	8	Interconnect Modeling II		
10/3	9	Fabrication I	PS 5	PS 4
10/8	10	Fabrication II		
10/10	11	Layout Rules	PS 6	PS 5
10/15	12	Inverter Properties		
10/17	13	Inverter Design I		PS 6
10/22	14	Inverter Design II	PS 7	
10/24		MIDTERM		
10/29	15	Logic Circuit Properties		
10/31	16	Logic Circuit Design I	PS 8	PS 7
11/5		NO CLASSES		
11/7	17	Logic Circuit Design II	PS 9	PS 8
11/12	18	Logic Circuit Optimization I		
11/14	19	Logic Circuit Optimization II	PS 10	PS 9
11/19	20	Clocking		
11/21	21	Latch Design	Proj	PS 10
11/26	22	Data Paths I		
11/28	23	Data Paths II		
12/3	24	Control - PLAs		
12/5	25	Memory Arrays I		
12/10	26	Memory Arrays II		Proj
12/17		FINAL EXAM (AM)		