High Performance GaInP/GaAs HBT Radio Frequency Integrated Circuits at 5 GHz (Invited Paper)

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Abstract— **Several high performance GaInP/GaAs heterojunction bipolar transistor (HBT) radio frequency integrated circuits (RFICs) implemented by our research group are reviewed in this paper. These demonstarted RFICs include source inductively degenerated cascode low noise amplifiers with inter-stage matching, shunt-series shunt-shunt dual feedback wideband amplifiers, broad band Gilbert down-conversion micromixer, Gilbert down-conversion mixers with poly-phase filters for image rejection, Gilbert up-conversion mixers with output LC current mirror and quadrature VCOs. In addition, a method to extract the GaInP/GaAs HBT device structure is also developed.**

I. INTRODUCTION

Commercially available 5 GHz WLAN transceivers except power amplifiers (PAs) have been using advanced CMOS and SiGe BiCMOS technology recently [1]. It is commonly believed that RFICs made by Si technology especially CMOS technology have the best cost and can be easily integrated with digital CMOS ICs to form a wireless system on chip (SOC). CMOS transceivers integrated with the digital CMOS ICs have been successfully demonstrated. It is the integration that makes the silicon technology attractive. However, it is still difficult to integrate the high power PA with the RF transceiver. There exist stand-alone high power CMOS PAs for cellular applications and low-end SiGe PAs integrated with RF transceiver for 2.4 GHz WLAN applications. The strong coupling in the Si substrate prevents the integrating power amplifier with the RF transceiver. Thus, the PAs at 5 GHz are stand-alone and dominated by the GaAs technology. 5 GHz GaInP/GaAs HBT WLAN PAs are commercially available now. As the CMOS device scaling by deep submicron technology continues, the cost of fabrication becomes very high and the device operating voltage decreases. Thus, the integration of high power amplifiers with the SOC becomes more difficult. Moreover, the size of RFICs does not follow the scaling rule as the digital IC does. It is worthwhile to mention that the cost of research and development for the deep submicron CMOS IC design has increased dramatically due to the high cost photo masks. The high R&D cost has set a big barrier for many companies to enter the wireless IC markets. GaInP/GaAs HBT PAs are made by very low cost 2 um photolithography. The cost for photo masks with 2 um accuracy is much lower than that for photo masks with 0.13 um accuracy. Thus, the IC design R&D cost for HBT technology is significantly lower than that for deep submicron CMOS technology. GaInP/GaAs HBT technology needs only roughly 10 mask steps while CMOS technology has more than 20 mask steps. There already exist 6-inch GaAs fabs compared with the 12-inch Si fabs. Thus, there is a chance that the production cost for GaAs HBT RF transceivers can be lower than that for CMOS RF transceivers. If the external GaInP/GaAs HBT PA is still unavoidable, it is straightforward to think of the possibility of integrating the whole transceiver including PAs in GaInP/GaAs HBT technology. The semi-insulating GaAs substrate eliminate the cross coupling between the PA with the RF transceiver.

The Program of Promoting Academic Excellence for Universities Phase II, funded by Ministry of Education of Taiwan, R.O.C. has supported our group to design and implement various key RFIC components using GaInP/GaAs HBT technology. RF transceivers contain many key components such as LNAs, mixers, wideband amplifiers and VCOs as shown in Fig. 1. In this paper, many GaInP/GaAs HBT RFIC building blocks except PAs for 5 GHz applications are presented because 5 GHz GaInP/GaAs HBT PAs are commercially available. A method to extract and monitor the GaInP/GaAs HBT device structure has also been developed by our group. More detailed information about the circuit performance and device characterization can be found in the references given.

II. THE GAINP/GAAS HBT TECHNOLOGY

The GaInP/GaAs HBT technology used here provides 2um emitter width transistors, and the device exhibits a 40 GHz peak cut-off frequency with 12V BV_{CEO}. This HBT technology also provides thin-film resistors, metal-insulator-metal capacitors, inductors and two-layer interconnect metals on semi-insulating substrate.

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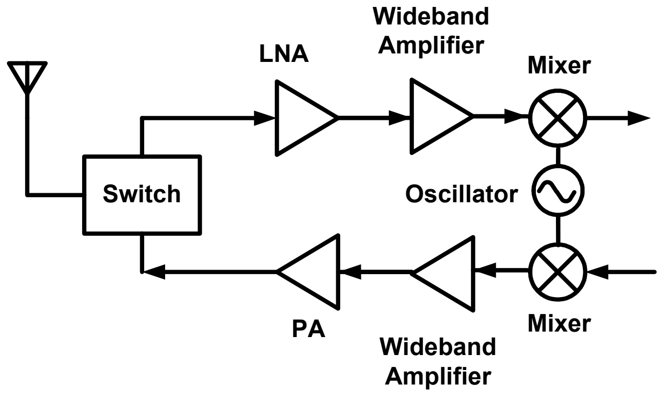

Fig. 1 The block diagram of a wireless transceiver including the power amplifier.

III. THE IMPLEMENTATION OF LOW NOISE AMPLIFIER AND WIDEBAND AMPLIFIER

A cascode LNA with source inductive degeneration is designed. The small signal gain can be increased by using inter-stage matching between the common emitter and common base transistors. It is possible to perform the impedance transformation in the inter-stage of a cascode amplifier for better transducer power gain. The 2 μm GaInP/GaAs HBT LNA without inter-stage matching has 14 dB power gain and 2.37 dB noise figure at 5.2 GHz while the 2 μm GaInP/GaAs HBT LNA with inter-stage matching has 19.5 dB power gain and 2.22 dB noise figure at 5.2 GHz. The circuit is biased at 3.6 V with the current consumption of 2.3 mA.

The shunt-series shunt-shunt dual feedback wideband amplifier [2][3] is the most popular topology for RF gain building block. The design methodology of the wideband amplifier has been developed by identifying poles and zeros of the wideband amplifier [4][5][6]. The shunt-series shunt-shunt wideband amplifier is a high speed Cherry-Hopper amplifier with a global shunt-series feedback. The experimental results showed that a small signal gain of 16 dB and a 3-dB bandwidth of 11.6 GHz with in-band input/output return loss less than 10 dB have been obtained. These values agreed well with those predicted from the analytic expressions that were derived for voltage gain, bandwidth, input and output impedances.

The design trade-off between gain bandwidth and matching bandwidth using emitter capacitive gain peaking is also demonstrated [7]. Experimental results show that power gain is 28 dB and input/output return loss is better than 12 dB from DC to 6 GHz for the wideband amplifier without emitter capacitive gain peaking. On the other hand, the wideband amplifier with emitter capacitive gain peaking has the same gain but the power gain bandwidth increases up to 8 GHz at the cost of lower input/output return loss. Power and noise performance are very similar for both types of wideband amplifiers. Both circuits have 8 dBm OP_{1dB} and 20 dBm OIP_3 at 2.4 GHz. Noise Figure of both designs are below 2.8 dB from 1 GHz to 6 GHz.

IV. THE IMPLEMENTATION OF DOWN-CONVERSION MIXER AND IMAGE REJECTION DOWN-CONVERTER

The micromixer proposed by Gilbert [8] [9] is an ideal circuit topology for active RF mixer designs. As shown in Fig.2, the micromixer consists of a common-emitter single balanced mixer, a common-base single balanced mixer, and a resistive degenerated current mirror. The micromixer can be view as an active balun that is able to generate differential signals from single-ended RF input. Since the GaInP/GaAs HBT technology provides semi-insulating substrate and metal-plated ground, the micro trip line structure is suitable for signal propagation. In other words, the RFIC using GaInP/GaAs HBT technology can operate well without differential operation. The micromixer is good because the input resistors in this topology achieve the input impedance matching and thus the chip area is saved.

A DC-8 GHz wideband GaInP/GaAs HBT micromixer is demonstrated [10]. Its conversion gain is 11 dB with resistive load and current injection technique. IP_{1dB} = -17 dBm and IIP_3 = -7 dBm are achieved for a small local oscillator power of –2 dBm when LO=5.35 GHz and RF=5.7 GHz.

The image signal suppression is a very important topic in RF receiver designs. The double quadrature down-converters with poly-phase filters are popular image rejection method for low-IF receivers [11] [12]. Figure 3 shows the block diagram of the image rejection down-converter. The demonstrated down-converter consists of four Gilbert mixers, and two passive four-section poly-phase filters. The desire signal and the image signal can be separated after mixed down by four Gilbert mixers. The IF poly-phase filters can then filter out the desired signal from the image signal. A 5.2 GHz 11 dB gain, IP_{1dB}= -17 dBm and IIP_3= -10 dBm double quadrature Gilbert downconversion mixer with polyphase filters [13] is demonstrated by using GaInP/GaAs HBT technology. The image rejection ratio is better than 40 dB when LO=5.17 GHz and IF is in the range of 15 MHz to 40 MHz.

V. THE IMPLEMENTATION OF UP-CONVERSION MIXER

A miniature lumped-element rat-race hybrid [14] and an LC current combiner are used in the LO port and the RF port of the up-conversion micromixer, respectively [15]. The fully integrated micromixer has conversion gain of 1 dB, OP_{1dB} of –10 dBm, and OIP_3 of 2 dBm when input IF=300 MHz, LO=4.9 GHz, and output RF=5.2 GHz. The output RF return loss is 23 dB at 5.2 GHz and the IF input return loss is better than 25 dB for frequencies up to 8 GHz.

In addition, the operation principle and the analytic function of the LC current combiner with the effect of the series resistor in an inductor are developed. The LC current combiner can be treated as a band-pass and passive current mirror load. Compared with low-pass and active current mirror load, the LC current combiner has better performance when the output frequency becoming higher. Therefore, the LC current combiner is an ideal topology to up-conversion mixer design.

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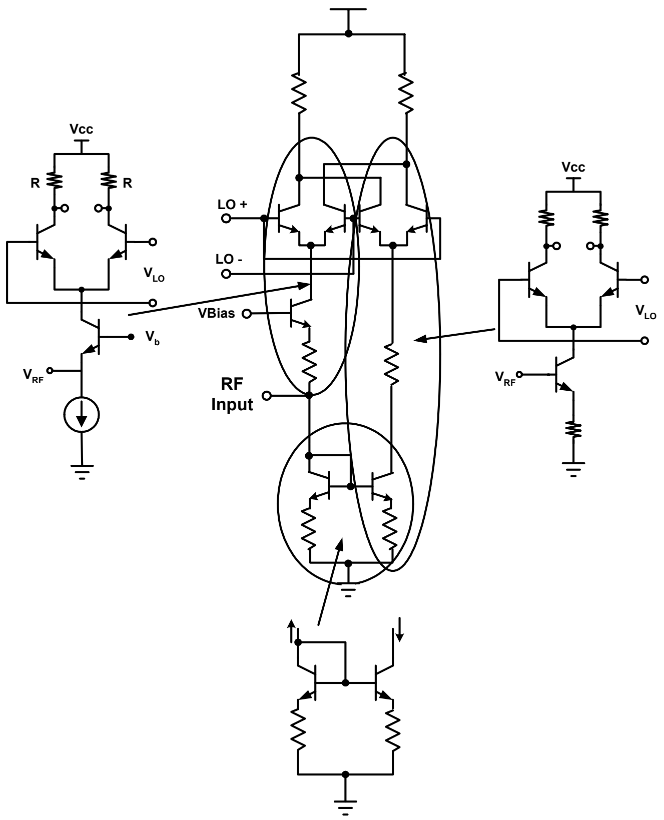

Fig. 2 The schematic of the micromixer topology.

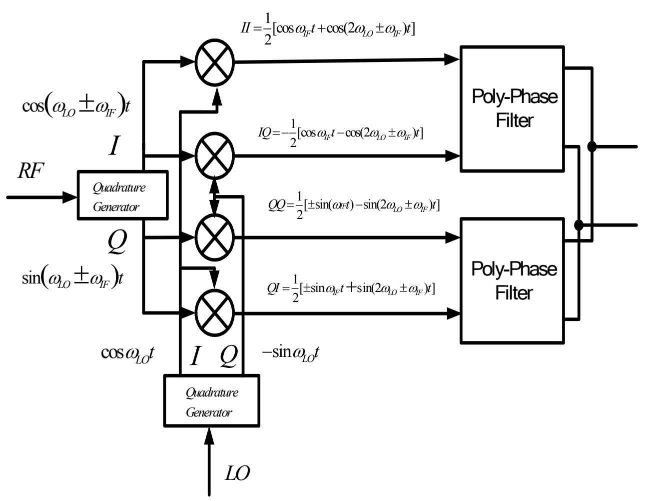

Fig. 3 The block diagram of double quadrature image rejection down-converter.

In RFIC design, the output node usually has to be lower down to low impedance since the RF 50 ohm low-impedance system. Traditionally, this can be easily achieved by using the common-collector output buffer. We found that the common-collector output buffer can provide power gain although it can not increase the voltage gain. The output buffer can be seen as a active matching network; moreover, the output buffer can perform conjugate matching at its input port and perform output 50 ohm matching. As a result, the power gain is increased and the output impedance matching is achieved at the same time.

An up-conversion micromixer with integrated VCO is also demonstrated [16]. A cross-coupled LC oscillator with oscillation frequency of 4.3 GHz and a cascode buffer amplifier are also integrated on the same chip. The fully integrated upconversion micromixer has conversion gain of -2.5 dB, OP_{1dB} of -12.5 dBm and 40 dB RF-IF isolation when input IF=0.9 GHz and thus output RF=5.2 GHz. The IF input return loss is better than 25 dB for frequencies up to 6 GHz while RF output return loss is better than 12 dB for frequencies from 5.15 GHz to 5.35 GHz.

VI. The Implementation of VCOs

GaInP/GaAs HBT quadrature VCO [17] is also implemented. A fully integrated GaInP/GaAs HBT quadrature VCO using the stacked-transformer LC tank is demonstrated [18] at 5.43-5.31 GHz with low-phase-noise performance. The GaInP/GaAs HBT device has small low-frequency noise because of the low base resistance, the suppression of trap-related 1/f noise by the device passivation ledge over the extrinsic base surface, and the absence of DX trap center in the GaInP material. A stacked transformer has the highest mutual coupling factor (close to one) between two spiral inductors [19] and the GaAs semi-insulating substrate results in a high self-resonant frequency for the stacked transformer. The quadrature VCO at 5.38 GHz has phase noise of -127.4 dBc/Hz at 1 MHz offset frequency, output power of -4 dBm and a figure of merit (FOM) -191 dBc/Hz.

The 5.7 GHz interpolative VCO with wide tuning range is demonstrated [20] [21]. Frequency tuning is achieved by interpolate two fixed oscillators instead of changing the tank capacitor. The demonstrated tuning range is 500 MHz.

VII. HBT Device Parameter Extraction

For the RFIC designers, it is very important to know and monitor the device structures for performance optimization. A method to extract the GaInP/GaAs HBT device structure has been developed and gives the designer the insight of the property of GaInP/GaAs HBT. The base thickness and base doping density are obtained through base transit time and base sheet resistance measurements while the base transit time is measured through the cut-off frequency measurements at various bias points. A large size two-emitter HBT device is used to measure the ledge thickness. The large size HBT device through C-V measurements obtains emitter doping profile and collector doping profile. An FATFET device formed by two emitters as drain and source terminals and the interconnect metal as the on-ledge Schottky gate between two emitters is used to measure the ledge thickness. [22].

VIII. Conclusion

Several key RFIC building blocks including LNA, wideband amplifier, up/down-conversion micromixer, image rejection down-converter, and VCOs are designed and implemented

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using the 2um GaInP/GaAs HBT technology. In addition, a powerful HBT device structure extraction method has been developed. The GaInP/GaAs HBT technology is suitable for RFIC design, and the future task is to merge these RF building blocks into a fully integrated RF transceiver.

ACKNOWLEDGMENT

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REFERENCES

[1] T. H. Lee, H. Samavati and H. R. Pategh, "5-GHz CMOS wireless LANs," IEEE Trans. Microwave Theory Tech., vol. 48, pp. 170-181, Feb 2000.

[2] R. G. Meyer and R. A. Blauschild, "A 4-terminal wide-band monolithic amplifier, "*IEEE J. Solid-State Circuits,* vol.sc-16, pp.634-638, Dec. 1981.

[3] C. D. Hull and G. B. Meyer, "Principles of monolithic wideband feedback amplifier design, "*Int. J. High Speed Electronics*, vol.3, pp.53-93, Feb.1992.

[4] M. C. Chiang, S. S. Lu, C. C. Meng, S. A. Yu, S. C. Yang, and Y. J. Chan "Analysis, design, and optimization of GaInP-GaAs HBT matched-impedance wide-band amplifiers with multiple feedback loops", *IEEE J. of solid-state circuits*, vol. 37, no. 6, pp. 694-701, June 2002.

[5] Shey-Shi Lu, Chin-Chun Meng, To-Wei Chen, and Hsiao-Chin Chen, "A novel interpretation of transistor S-parameters by poles and zeros for RF IC circuit design," *IEEE Transactions on Microwave Theory and Techniques*, Vol.49, pp406-409, Feb. 2001.

[6] S. S. Lu, C. C. Meng, T. W. Chen and H. C. Chen, "The origin of the kink phenomenon of transistor scattering parameter S22", IEEE transaction on microwave theory and techniques, Vol. 49, No.2, pp.333-340, Feb 2001.

[7] C. C. Meng, T. H.Wu and S. S. Lu, "28dB Gain DC-6GHz GaInP/GaAs HBT Wideband Amplifiers with and without Emitter Capacitive Peaking", *European gallium arsenide and other semiconductors application symposium (GAAS 2002)*, pp. 311-314, September 2002.

[8] B. Gilbert, "The MICROMIXER: A highly linear variant of the Gilbert mixer using a bisymmetric class-AB input stage," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1412-1423, Sept. 1997.

[9] J. Durec and E. Main, "A linear class AB single-ended to differential transconverter suitable for RF circuits," *IEEE MTT-S Int. Microwave Symp. Dig*., vol. 2, June 1996, pp. 1071-1074.

[10] C. C. Meng, S. S. Lu, M. H. Chiang, and H. C. Chen, "DC to 8 GHz 11 dB gain Gilbert micromixer using GaInP/GaAs HBT technology", *Electronics Letters*, pp. 637-638, April 2003.

[11] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE J. of solid-state circuits*, vol. 36, no. 6, June 2001.

[12] J. Crols and M. Steyaert, "A Single-Chip 900 MHz CMOS Receiver Front-End with a High Performance Low-IF Topology," *IEEE J. of Solid-State Circuits*, vol. 30, no. 12, pp. 1483-1492, Dec. 1995.

[13] C. C. Meng, D. W. Sung, and G. W. Huang, "A 5.2 GHz GaInP/GaAs HBT double quadrature downconverter with polyphase filters for 40 dB image rejection", *IEEE microwave and wireless components letters*, vol. 15, no. 2, pp. 59-61, Feburary 2005.

[14] S. J. Parisi, "180^{o} lumped element hybrid", *IEEE MTT-S international microwave symposium,* pp. 1243-1246, 1989.

[15] C. C. Meng, T. H. Wu and M. C. Lin, "Compact 5.2-GHz GaInP/GaAs HBT Gilbert upconverter using lumped rat-race hybrid and current combiner," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 10, Oct 2005.

[16] C. C. Meng, S. K. Hsu, A. S. Peng, S. Y. Wen, and G. W. Huang, "A fully integrated 5.2 GHz GaInP/GaAs HBT upconversion micromixer with output LC current combiner and oscillator", *IEEE MTT-S Digest*, 2003, vol 1, pp. A205-A208.

[17] P. Andreani, "A low-phase-noise, low-phase error, 1.8 GHz quadrature CMOS VCO", *Proc. ISSCC* 2002, pp. 290-291, February 2002.

[18] C. C. Meng, C. H. Chen, Y. W. Chang, and G. W. Huang, "5.4 GHz -127 dBc/Hz at 1 MHz GaInP/GaAs HBT quadrature VCO using stacked transformers", *Electronics Letters*, vol. 41, no. 16, pp. 906-908, August 2005.

[19] Zannoth, M., Kolb, B., Fenk, J., and Weigel, R., 'A fully integrated VCO at 2 GHz', *IEEE J. Solid-State Circuits*, 1998, **33**, (12), pp. 1987-1991

[20] N. M. Nguyen and R. G. Meyer, "A 1.8-GHz Monolithic LC Voltage-Controlled Oscillator," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 444-450, Mar. 1992.

[21] S. A. Yu, C. C. Meng, and S. S. Lu, "A 5.7 GHz interpolative VCO using GaInP/GaAs HBT Technology", *IEEE microwave and wireless components letters*, vol. 12 no. 2, pp. 37-38, Feburary 2002

[22] C. C. Meng, B. C. Tsou, and S. C. Tseng, "Determining GaInP/GaAs HBT Device Structure by DC Measurements on a Two-Emitter HBT Device and High Frequency Transit Time Measurements", *IEICE Trans. Electron.*, vol.E88-C, no.6, June, 2005.

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