

Noise and Power Reduction in Filters Through the Use of Adjustable Biasing

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Abstract—A technique that enables the variation of bias currents in a filter without causing disturbances at the output is presented. Thus, the bias current can be kept at the minimum value necessary for the total input signal being processed, reducing the noise and power consumption. To demonstrate this approach, a dynamically biased log-domain filter has been designed in a 0.25- μm BiCMOS technology. The chip occupies 0.52 mm². In its quiescent condition, the filter consumes 575 μW and has an output noise of 4.4 nA rms. Signal-to-noise ratio greater than 50 dB over 3 decades of input and total harmonic distortion less than 1% for inputs less than 2.5 mA peak are achieved. The bias can be varied to minimize noise and power consumption without disturbing the output.

Index Terms—Analog filters, companding, dynamic bias, log-domain.

I. MOTIVATION AND PRINCIPLE OF THE PROPOSED TECHNIQUE

A. Bias Current, Noise, and Power Consumption of Filters

ANALOG active filters, shown in a general form in Fig. 1(a), typically consist of an interconnection of active elements, capacitors, resistors and bias currents. The output noise and the power dissipation of the filter are determined by the bias currents used inside the filter. In a conventional filter, the bias currents are constant with respect to variations in the strength of the input and are designed to be large enough to accommodate the current swings due to the largest input signal. In Fig. 1(b), the output signal and the output noise of a conventional filter are plotted versus the input signal on a logarithmic scale. The output noise N is a constant, owing to the constant internal bias currents. The output signal S is directly proportional to the input signal. The vertical separation between the curves is the signal-to-noise ratio (S/N). The largest input signal that can be applied to the filter is marked on the figure. The S/N of the filter is highest when the input is at its maximum value. S/N decreases in direct proportion to the input signal as the latter is decreased from its maximum value. The power dissipation is also a constant with respect to variations in the input amplitude and is qualitatively depicted in Fig. 1(c). Since the bias currents are designed to handle the largest input signal, the power consumption and the noise of the filter are unnecessarily large when smaller signals are present.

A more favorable situation is shown in Fig. 2. Fig. 2(a) shows the general form of a filter in which the bias currents are vari-

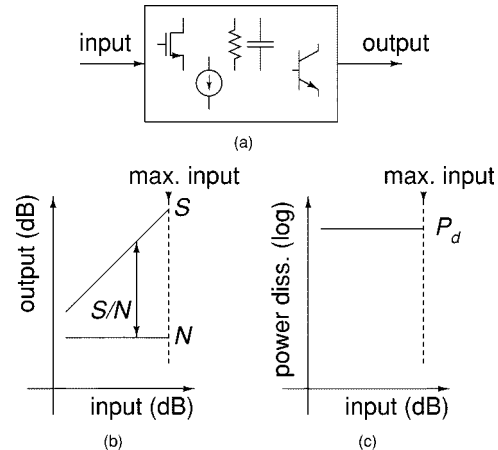


Fig. 1. Analog filter with constant bias currents. (a) General form. (b) Signal and noise. (c) Power dissipation.

able by means of an external control. As the amplitude of the input signal decreases, the bias currents can be decreased in order to reduce the noise and the power consumption of the filter. Fig. 2(b) shows the output signal and the output noise of the filter versus the input signal level. Owing to the signal dependent bias, the output noise N decreases as the input signal is decreased from its maximum value. The S/N , which is given by the vertical separation between the two curves, is better in comparison to the previous case [Fig. 1(b)] for inputs that are smaller than the maximum limit. Similarly, the power consumption [Fig. 2(c)] is smaller when compared to the case with a constant bias current.

It was mentioned previously that the noise of a filter can be reduced by decreasing the bias currents. This may seem contradictory to the general impression that low-noise circuits require larger currents and hence, a larger power dissipation. However, larger currents are required only to improve the *maximum signal-to-noise ratio* of a circuit. If only a reduction in noise is desired, it can be achieved by lowering the bias current. Lowering the bias current in this manner would also reduce the maximum signal that can be handled by the circuit. This is not a problem as the bias current is intended to be lowered only when the input signal is small.

B. Realizing Filters With Dynamically Adjustable Bias

The bias currents determine the time constants of a filter in addition to its noise and power consumption. Therefore, varying the bias currents changes the transfer function of the filter in addition to its power consumption and noise, which is wholly undesirable. This makes it nontrivial to realize filters with a dy-

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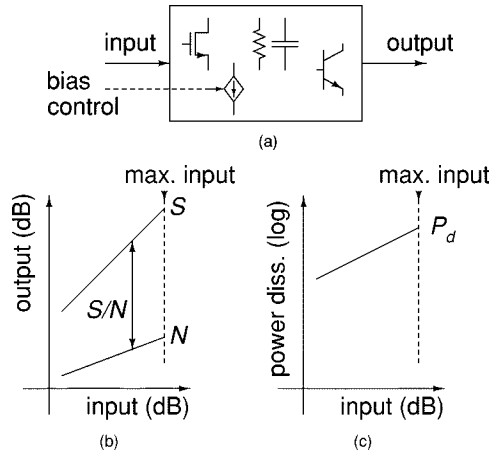


Fig. 2. Analog filter with variable bias currents. (a) General form. (b) Signal and noise. (c) Power dissipation.

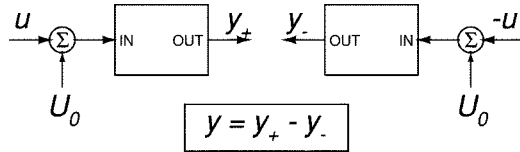


Fig. 3. Pseudodifferential operation of externally linear filters with bias added at the input.

namically adjustable bias. This has been discussed for the case of $g_m - C$ filters in [1].

For certain types of filters in which the internal bias currents can be controlled from the input and which are large-signal linear from the input to the output, dynamic adjustment of the bias can be accomplished as shown in Fig. 3. The system consists of two filters which are input–output linear. The input signal and the bias are added and fed to each of the filters. Both filters receive the same bias U_0 (which can be time varying) and opposite inputs u and $-u$. The outputs of the two filters are given by

$$y_+(t) = (u(t) + U_0(t)) * h(t) \quad (1)$$

$$y_-(t) = (-u(t) + U_0(t)) * h(t) \quad (2)$$

where $h(t)$ is the impulse response of the input–output linear filter and $*$ denotes convolution. The overall output y is defined to be the difference of the individual outputs and is given by

$$y = y_+ - y_- \quad (3)$$

$$= 2u(t) * h(t). \quad (4)$$

The time-varying bias U_0 disappears in the difference output and can be adjusted as required to optimize the noise and power consumption of the filter. The realization of such a filter is given in Section II.

C. Limitations of the Proposed Technique

The bias currents of the filter described above are adjusted based on the total input signal including its in-band and out-of-band components. If a small in-band signal were to be accompanied by a large out-of-band signal, based on the latter, the bias currents would be set to a large value. This results in a

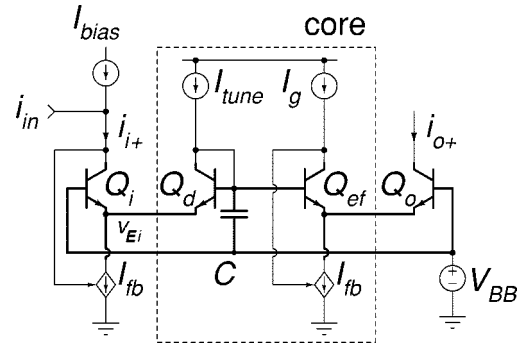


Fig. 4. First-order log-domain filter.

larger noise and power dissipation than in a situation without the large out-of-band signal. Therefore, for applications in which the difference between the out-of-band and in-band signal is very large, dynamic biasing does not improve the S/N for small input signals. It still provides the ability to handle a large signal while keeping the quiescent power dissipation small.

II. PRACTICAL REALIZATION

A. Log-Domain Filter

It was mentioned above that the technique of Fig. 3 can be used when the internal bias can be controlled from the input. Log-domain filters [2]–[5] have this property and will be used here to illustrate the principle. Fig. 4 shows a first-order log-domain filter [4]. Desired currents are forced into Q_i and Q_{ef} using feedback-controlled current sources I_{fb} around them. V_{BB} is a constant voltage bias. The input transistor Q_i converts the current i_{i+} into a logarithmically related voltage V_{Ei} at its emitter. The diode-connected transistor Q_d and the capacitor C perform nonlinear filtering of the logarithmically compressed voltage. The capacitor voltage is level shifted by the transistor Q_{ef} , which is biased at a constant current I_g . The level-shifted voltage is exponentially converted to the output current i_{o+} by the transistor Q_o . The filter can be viewed as 1) a nonlinear filter core between a logarithmic current-to-voltage and an exponential voltage-to-current converter [2]–[4], or 2) as a dynamic translinear loop of base–emitter junctions of bipolar transistors and capacitors [6]. In either case, assuming $i_{i+} > 0$ and that the bipolar transistors follow the exponential relationship between their base–emitter voltages and collector currents, it can be shown that the filter in Fig. 4 is *large-signal* linear between the currents i_{i+} and i_{o+} , although the internal voltages and currents are nonlinearly related to i_{i+} . i_{i+} and i_{o+} are related in the time domain by

$$\frac{di_{o+}}{dt} = -\frac{I_{tune}}{CV_t}i_{o+} + \frac{I_g}{CV_t}i_{i+}. \quad (5)$$

The equivalent relation in the frequency domain is

$$\frac{I_{o+}}{I_{i+}} = \frac{I_g/I_{tune}}{1 + sCV_t/I_{tune}} \quad (6)$$

$$= \frac{k}{1 + s/\omega_p}. \quad (7)$$

The currents I_g and I_{tune} and the capacitor C determine the dc gain k and the pole ω_p of the filter.

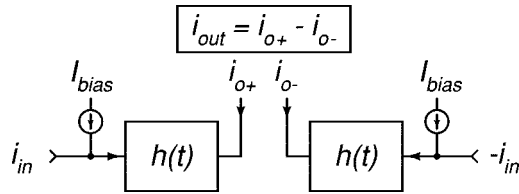


Fig. 5. Pseudodifferential operation for distortionless dynamic biasing.

The total input current i_{i+} in Fig. 4 is the sum of a signal current i_{in} and a dc bias I_{bias} . With $i_{in} = 0$, the integrated output noise $i_{n,o+}$ (due to collector shot noise of Q_{1p-4p}) is given by¹

$$i_{n,o+}^2 = \frac{q\omega_p}{2}(k + k^2) \left(I_{bias} + \frac{I_{bias}^2}{I_{tune}} \right). \quad (8)$$

The bias current I_{bias} affects the output noise but not the transfer function (6). I_{bias} also limits the maximum negative swing of the input current i_{in} . I_{bias} can be varied in accordance with the envelope of the input i_{in} so that it is slightly larger than the minimum value required in order to maintain a positive i_{i+} at all times [7]. Such a biasing arrangement lowers the power consumption and the output noise of the filter for small inputs and, at the other extreme, can accommodate very large inputs. However, a time-varying $I_{bias}(t)$ results in transients in the current i_{o+} of the output transistor Q_o . This problem can be overcome using pseudodifferential operation of the filters, as shown earlier in Fig. 3. The single-ended filter shown in Fig. 4 is duplicated and operated with the same bias I_{bias} but an opposite input signal $-i_{in}$ (Fig. 5), [8]. The bias current disappears in the difference output due to the large signal linearity of the filters. The relation between i_{in} and i_{out} is linear and time-invariant. Therefore the bias current I_{bias} can be adjusted to minimize the output noise and the power consumption of the filter without disturbing the output.

Syllabic companding (see [11], [12] and the references therein) is a technique used to extend the input range of the filter using variable gain amplifiers at the input and the output which are adjusted to maintain constant internal swings despite changes in the input signal amplitude, without causing disturbances in the output signal. Dynamic biasing accomplishes the same without requiring explicit amplifiers at the input and the output. The emitter voltage V_{Ei} of the input transistor Q_i in Fig. 4 is given by

$$V_{Ei}(t) = V_{BB} - V_t \ln \frac{i_{in}(t) + I_{bias}}{I_s} \quad (9)$$

where I_s is the saturation current and V_t is the thermal voltage. Assume that the input signal increases by a factor α to $\alpha i_{in}(t)$ and that the biasing arrangement increases the bias current by the same factor α to $\alpha I_{bias}(t)$. The emitter voltage V_{Ei} then changes to

$$V_{Ei}(t) = V_{BB} - V_t \ln \frac{\alpha i_{in}(t) + \alpha I_{bias}}{I_s} \quad (10)$$

$$= V_{BB} - V_t \ln \frac{i_{in}(t) + I_{bias}}{I_s} - V_t \ln \alpha. \quad (11)$$

¹The noise from Q_o is not bandlimited. Its spectral density is multiplied by the noise bandwidth of the low-pass filter ($0.25\omega_p$ Hz) in order to obtain (8)

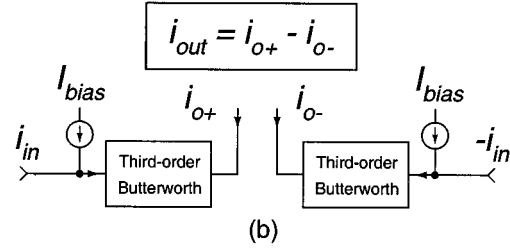
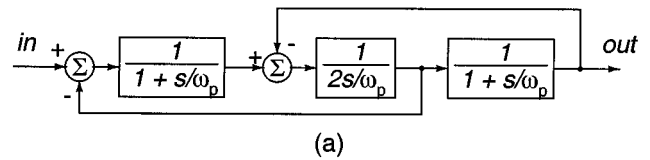


Fig. 6. (a) Block diagram of the third-order Butterworth filter. (b) Pseudodifferential version.

The voltage V_{Ei} which is fed to the core of the filter experiences only a dc shift $V_t \ln \alpha$. The “ac” part remains the same, just as it would with syllabic companding.

When the internal state-variable description of a log-domain filter is available, the technique of operating two filters in a pseudodifferential mode can also be derived using the approach in [9]. Pseudodifferential log-domain filters also are used in [10] to implement *instantaneously companding* filters. Although the system in Fig. 3 may be topologically similar to the circuits presented in [10], the objective here is syllabic companding.

B. Third-Order Butterworth Log-Domain Filter

A third-order Butterworth low-pass filter with a 1-MHz bandwidth is used to evaluate the proposed technique. The leapfrog realization shown in Fig. 6(a) is the prototype for the current design. The pseudodifferential filter is shown in Fig. 6(b). It consists of two identical single-ended third-order filters fed with the same bias I_{bias} and opposite inputs i_{in} and $-i_{in}$.

Fig. 7(a) shows the simplified schematic of the single-ended third-order filter. The general structure is similar to that of the first-order filter in Fig. 4. An input transistor Q_i converts the current i_{i+} into a logarithmically compressed voltage at its emitter. This voltage is fed to the core of the filter, which consists of three sections. Each section is similar to the first-order filter core in Fig. 4. The output voltage of the core is converted to an exponentially related current by the output transistor Q_o .

Each section of the core is shown in some detail in Fig. 7(b). The current I_{tune} and the capacitor C determine the time constant, and I_g determines the gain of the particular section. The input voltages to the section are fed to the emitters of the bipolar transistors. Depending on the sign of the input, their collector currents are either driven into (using a current mirror) or drawn out of the capacitor C [4]. The capacitor voltage is level shifted using the emitter follower Q_{ef} .

The schematic of the single-ended filter is shown in Fig. 7(c). The three stages of the filter are marked. The feedback to the first two stages can be clearly seen. I_{tune} is absent from the second stage since the latter is a lossless integrator [Fig. 6(a)]. To realize a bandwidth of 1 MHz, the following values are used in Fig. 7(c): $C_1 = C_3 = 30$ pF, $C_2 = 60$ pF, and $I_{tune} = I_g = 5$ μ A.

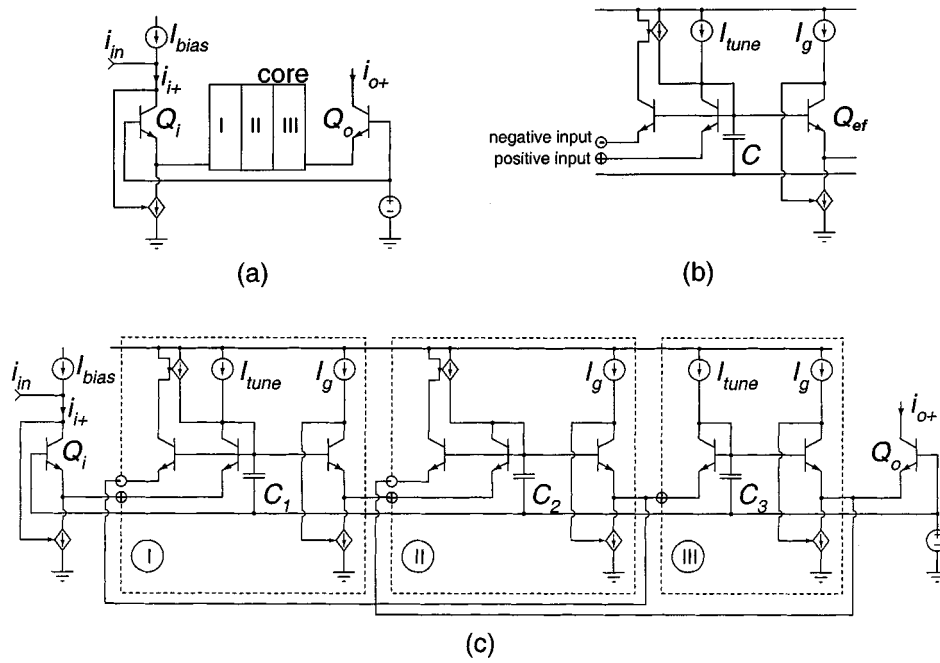


Fig. 7. (a) Simplified schematic of the single-ended third-order filter. (b) One section of the filter. (c) Schematic of the single-ended filter (further details are in Figs. 8-10).

The operation of the log-domain filter is based on the exponential relationship between the base-emitter voltage and the collector current of the bipolar transistor. Any deviation from the exponential behavior results in distortion at the output. Some causes of deviation from the exponential behavior are the emitter resistance, the base resistance, and the Early effect. In the technology available to us, the finite output resistance of the transistors due to Early effect was the dominant cause of distortion over most of the intended range of bias currents.

To combat distortion due to Early effect, the collector-emitter voltage swings of the bipolar transistors must be minimized. Fig. 8(a) shows the feedback arrangement used to force the current i_{i+} into the collector of the transistor Q_i . The collector-emitter voltage swing of Q_i is small if the transconductance of the feedback current source I_{fb} is large. To obtain the largest transconductance for a given current, a bipolar transistor Q_f is used to realize I_{fb} as shown in Fig. 8(b). A source follower M_f is used to drive Q_f in order to ensure a sufficient voltage across the transistors Q_i and Q_f , and, to prevent the base current of Q_f from being drawn out of the input node. With the source follower, the feedback loop consists of three poles, and is prone to instability, especially at small values of I_{bias} . A capacitor C_c is used to bypass M_f for high frequencies and compensate the loop. C_c is realized using an nMOS transistor operating in inversion.

The finite output resistance of the current sources (I_{tune} and I_g) and the current mirrors used in the circuit [Fig. 7(c)] have the same effect as the finite output resistance of the bipolar transistors. To minimize the consequent distortion, cascode structures with relatively long channels are used for the current sources and the current mirrors in the circuit. The use of long channels also reduces the $1/f$ noise from the current sources and the current mirrors.

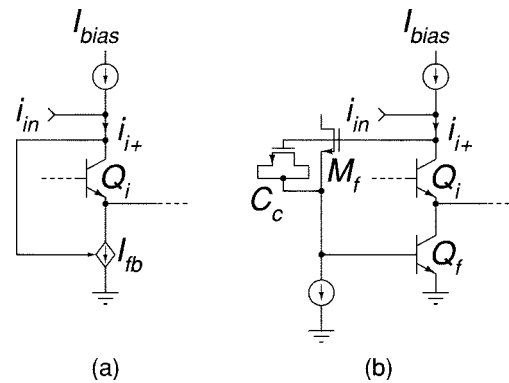


Fig. 8. Feedback circuit used to force a current into the collector.

The relation between the base-emitter voltage and collector current of a transistor deviates from the exponential at high current densities due to increased voltage drop across the parasitic series resistances and high-level injection effects. At very low current densities—i.e., with a very large transistor for a given current—the high-frequency response of the transistor deteriorates due to larger parasitic capacitances. The transistors in the log-domain filter are sized to strike a compromise between these two conflicting requirements. The currents in the input and the output transistors of a dynamically biased filter can be much higher than those in the core. For this reason, the input and the output transistors (Q_i and Q_o) in the filter are made four times larger than the transistors in the filter's core (Fig. 9). Increasing the size of both the input and the output transistors in the same proportion leaves the transfer function of the filter unaffected.

The leapfrog realization of the Butterworth filter consists of two feedback loops. The overall frequency response of the filter is very sensitive to parasitic phase shifts in these feedback paths. The realization of the feedback path from the third integrator in

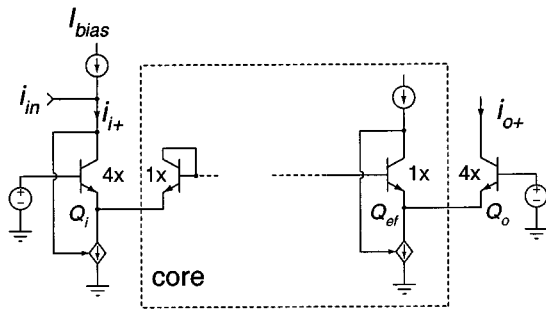


Fig. 9. Transistor sizing in the input and the output stages.

the log-domain filter is shown in Fig. 10(a). The emitter follower transistor Q_{ef} drives the feedback transistor Q_{fb} in addition to the output transistor Q_o . The emitter follower's load varies widely as the current in the output transistor varies over a large range due to dynamic biasing. This causes phase variations² between the emitter follower's input and output. Due to these phase shifts, the transfer function of the filter varies greatly with the bias current. To prevent this, the emitter follower Q_{ef} is split in two transistors Q_{ef1} and Q_{ef2} which separately drive the output and feedback paths, respectively [Fig. 10(b)]. In this case, the widely varying load is outside the feedback loop and simulations show that the desired frequency response is maintained over the intended range of bias currents.

III. MEASURED RESULTS

The pseudodifferential third-order Butterworth filter is fabricated in a 0.25- μm BiCMOS technology. Fig. 11 shows the chip photograph. The filter, excluding pads, occupies 0.52 mm² of which 0.38 mm² is used by the metal-metal capacitors.

All measurements are done with a supply voltage of 2.5 V. The current I_{tune} which controls the bandwidth is set to the design value of 5 μA . Fig. 12 shows the measured frequency response between the differential input and the differential output of the filter. The various curves correspond to different bias currents (I_{bias}) between 3 μA –2.5 mA. The response from the common-mode input to the differential output is also shown. Due to mismatches in the two pseudodifferential paths, there is imperfect cancellation of the common-mode input in the differential output. In the passband, the differential output due to the common-mode input is at least 35 dB below that due the differential input. In a dynamically biased filter, this represents the amount of “dynamic bias” that leaks to the output. The inset in Fig. 12 shows the passband detail of the frequency response. As the bias current is varied, the dc gain of the filter varies by about 0.5 dB, but the 3-dB bandwidth of the filter stays nearly constant at 930 kHz.

The reason for this gain variation can be understood by examining Fig. 8(b). The collector-emitter voltage V_{CEi} of Q_i increases with increasing input bias current due to the increase in the base-emitter voltage of Q_f and the gate-source voltage of M_f .³ The base-emitter voltage V_{BEi} of transistor Q_i is given by $V_{BEi} = V_t \ln[i_{i+}/I_s(1 + V_{CEi}/V_A)]$ where V_A is the Early

voltage of the bipolar transistor. For a given input i_{i+} , V_{BEi} decreases as V_{CEi} increases. The effect of finite Early voltage is an apparent scaling of the input signal by a factor $1/(1 + V_{CEi}/V_A)$. Therefore, as V_{CEi} increases with increasing input bias current, the gain of the filter decreases. A similar effect occurs in the output stage (Fig. 9) due to an increase in the collector-emitter voltage of the transistor Q_{ef} .

It was mentioned in Section I that the bias current I_{bias} in the proposed filter must be adjusted in accordance with the amplitude of the input signal i_{in} . The signal controlling the bias may be present in the system or may be derived from i_{in} using an envelope detector. For the following measurements, the bias current I_{bias} is manually set to twice the amplitude of the *single-ended* input i_{in} [Fig. 6(b)], unless that value was less than 3 μA , in which case I_{bias} was maintained at 3 μA . This is to mimic the action of the envelope detector operating on the input signal i_{in} . With such a bias adjustment, the measured rms values of the output signal and the noise in the differential output I_{out} are plotted versus the differential peak input in Fig. 13. The output noise spectral density is integrated up to 2 MHz to obtain the rms noise. With a 2.5-mA_{pk} input, the output noise is 1.5 μA_{rms} and decreases in near proportion to the input signal as the input is reduced. Below an input of 3 μA , the output noise remains constant at 4.4 nA_{rms} due to the constant bias current I_{bias} of 3 μA .

Fig. 14 shows the variation of the signal-to-noise and signal-to-distortion ratios versus the amplitude of the differential input signal with the bias current adjusted as described above. At an input amplitude of 2.5 mA, the S/N is 61 dB. Over a signal range of 3 decades below 2.5 mA, S/N varies slowly by about 10 dB. Below an input of 3 μA , where the bias current is no longer proportional to the input amplitude, S/N falls at the rate of 20 dB per decade as in a conventional linear filter.

In the ideal case, the output of a pseudodifferential filter should be free of second-harmonic distortion. But in our chip, due to mismatches, the second-harmonic distortion in fact dominated the third-harmonic distortion for bias currents up to 2.5 mA. The total harmonic distortion ($\text{THD} \approx \sqrt{\text{HD}_2^2 + \text{HD}_3^2}$) was measured using a 400-kHz tone at the input and adjustable biasing as described above. Fig. 14 shows the variation of THD with the differential input amplitude. For inputs below 0.8 mA, S/THD is more than 60 dB and shows little variation. The distortion increases sharply for input amplitudes larger than 1 mA due to increasing voltage swings in the circuit. S/THD is 41 dB for an input amplitude of 2.5 mA.

For intermodulation measurements, two tones separated by 40 kHz are fed to the input. Fig. 15 shows the ratio of the signal to the intermodulation distortion (S/IM_3) versus the center frequency of the two-tone input. In this measurement, the bias current I_{bias} is 200 μA and the single-ended input peak is 100 μA . The distortion increases monotonically with frequency due to increasing effect of the parasitic capacitances in the circuit.

The worst-case in-band intermodulation distortion is evaluated using inputs near the passband edge—two tones at 1 MHz \pm 20 kHz. Fig. 14 shows S/IM_3 plotted versus the differential input amplitude. The bias current I_{bias} is set based on the input amplitude, as described previously. For input

²There are gain variations as well, but they do not have as severe an effect.

³This is due to body effect and increasing drain current caused by the increasing base current of Q_f .

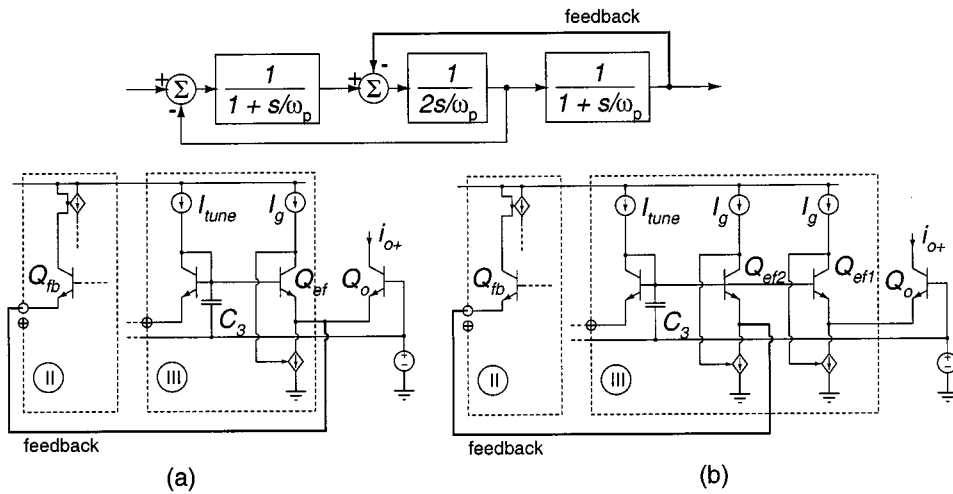


Fig. 10. Minimizing the bias dependent phase shift in the feedback path.

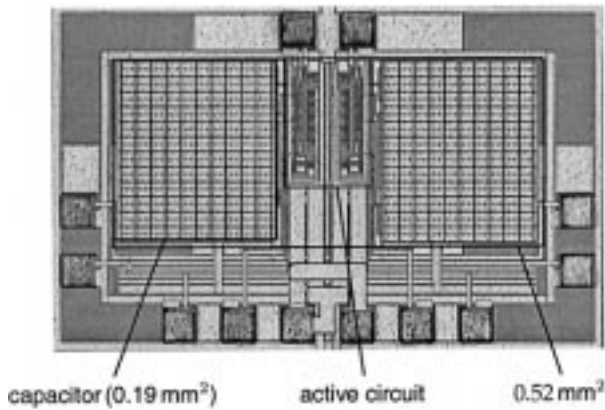


Fig. 11. Chip photograph.

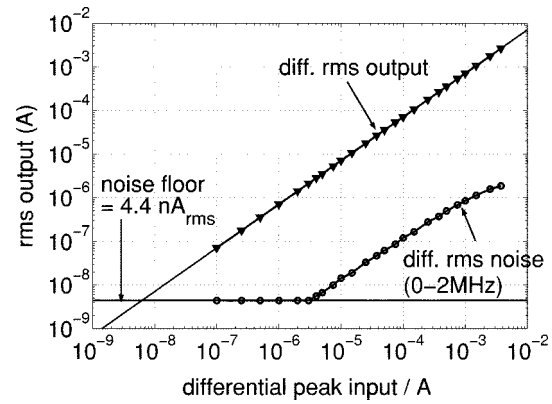


Fig. 13. Measured output signal and noise.

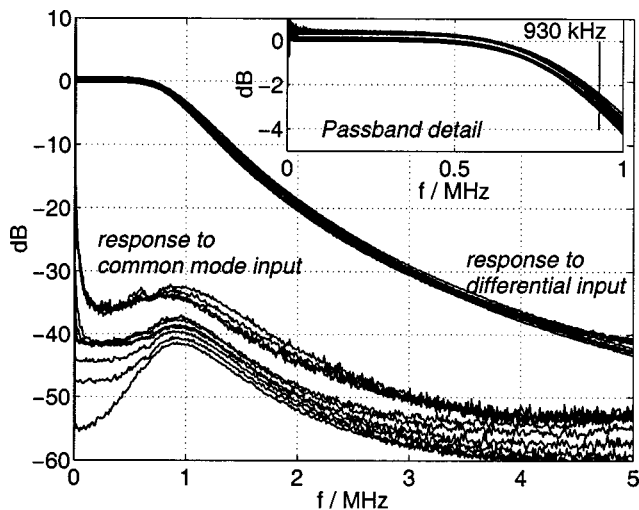


Fig. 12. Measured frequency response. I_{bias} from $3 \mu A$ to $2.5 \mu A$.

amplitudes above $10 \mu A$, the variation of the intermodulation distortion is similar to that of the harmonic distortion. As the input (and the bias current I_{bias}) is reduced below $10 \mu A$, the parasitic capacitive admittances in the circuit become more significant when compared to the desired conductances and the intermodulation distortion increases. Below an input of

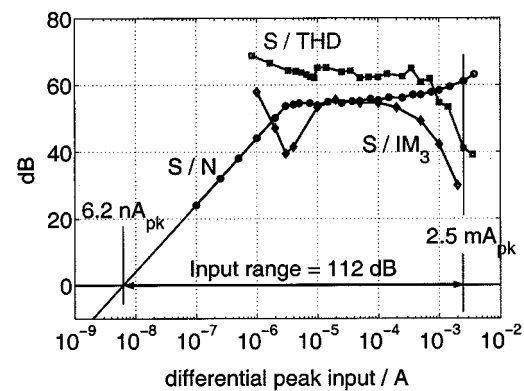


Fig. 14. Measured signal-to-noise and distortion ratios.

$3 \mu A$, the bias current I_{bias} is held constant, and therefore, the intermodulation distortion decreases with decreasing input amplitude, as it would in a conventional filter.

The extrapolated S/N reaches 0 dB at an input amplitude of 6.2 nA (Fig. 14). The total harmonic distortion is -41 dB for an input amplitude of 2.5 mA. The input range of the filter is defined to be between these two limits and is 112 dB. Such a large input range is due to input-dependent biasing which helps maintain a near-constant S/N as the input is decreased below the maximum limit.

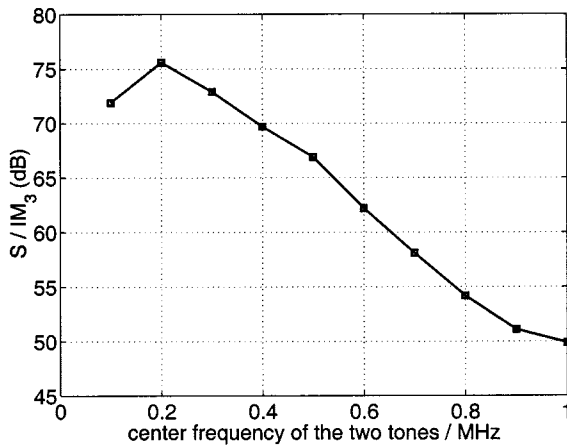


Fig. 15. Measured S/IM_3 versus frequency. IM_3 : two tones separated by 40 kHz. Combined input peak = $100 \mu A$. $I_{bias} = 200 \mu A$.

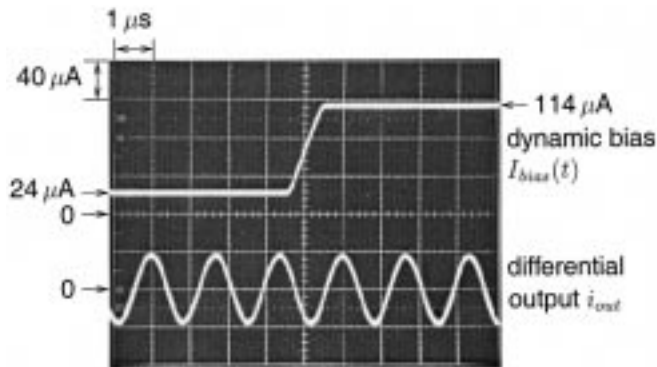


Fig. 16. Effect of a dynamically varying bias current $I_{bias}(t)$ on the differential output.

A test meant to verify the cancellation of bias transients is presented next. Fig. 16 shows the response of the filter to a 600-kHz sinusoid with a differential peak value of $40 \mu A$. Initially, the bias current I_{bias} is $24 \mu A$, which is 20% larger than the *single-ended* peak input. It is then increased to $114 \mu A$ in less than a microsecond. As seen, the output is practically unaffected by transients in I_{bias} , confirming the time invariance of the filter in presence of a time-varying I_{bias} .

With the bias current I_{bias} adjusted as described earlier, the measured current and power consumption of the filter are shown as a function of the differential input amplitude in Fig. 17. The quiescent power consumption is $575 \mu W$. At the maximum input of 2.5 mA_{pk} , the filter dissipates 26.1 mW . Table I summarizes the performance of the chip.

IV. COMPARISON

The last line in Table I is the maximum power dissipation of the filter normalized to the 3-dB bandwidth and the order. This serves as a normalized figure of merit that can be used to compare filters of different orders and bandwidths [13]. Table II lists the power dissipation, bandwidth, order, and input range of several previously published active filters and of the proposed filter. The input range specified is the range of input signals over which $THD \leq 40 \text{ dB}$ and $S/N > 0 \text{ dB}$ are maintained. Of

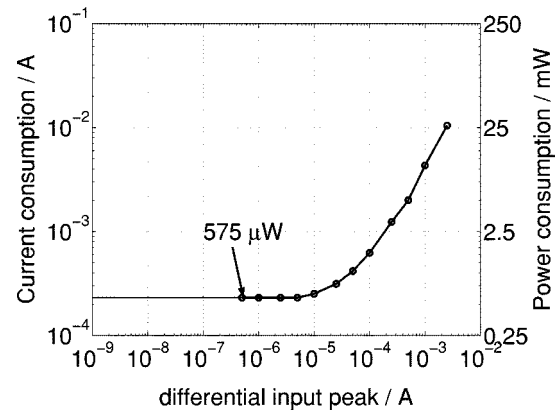


Fig. 17. Measured current and power consumption.

TABLE I
PERFORMANCE SUMMARY

Technology	0.25 μm BiCMOS	
Area (excl. pads)	0.52 mm ²	
Supply voltage	2.5 V	
3 dB BW	930 kHz	
I_{bias}	3 μA	2.5 mA
Power diss. (P_d)	575 μW	26.1 mW
Output noise	4.4 nA	1.5 μA
THD (input peak = $0.5I_{bias}$)	-64.3 dB	-41 dB
IM_3 (input peak = $0.5I_{bias}$)	-39.5 dB	-30 dB
Input range ($THD \leq -41 \text{ dB}$)	112 dB	
Maximum $P_d / \text{Order} \cdot \text{BW}$	9.35 nJ	

the listed filters, 3, 5, and 8 are log-domain class-AB filters and the rest are conventional linear filters. For the latter, the input range as defined above is also the S/N when the THD is 40 dB. To the best of the authors' knowledge, these are the filters with the largest input range per unit power consumption. The normalized power dissipation of the filters in Table II is plotted versus their input range in Fig. 18. The solid line corresponds to a first-order passive RC low-pass filter. It represents the power drawn by the RC filter from a sinusoidal input source whose frequency is equal to the filter's 3-dB bandwidth [13]. It reflects the well-known direct proportionality between the power dissipation and the input signal range. As seen, the point corresponding to the proposed filter is closer to the passive- RC line than previously published filters by nearly two orders of magnitude. This represents a corresponding improvement in the power efficiency of continuous-time filters.

This filter maintains $S/N > 0 \text{ dB}$ and $THD < 1\%$ for inputs over a 112-dB range. However, this filter is *not equivalent* to a conventional, internally linear filter with a 112 dB dynamic range. The latter would have a signal-to-noise ratio of 112 dB when its input signal at its maximum. However, the power dissipated in such a filter would be several orders of magnitude larger. The proposed filter is suitable for cases where a modest S/N and a near-optimum power dissipation must be maintained over a large range of input amplitudes.

TABLE II
POWER DISSIPATION PER S/N , SIGNAL FREQUENCY AND FILTER ORDER FOR PUBLISHED ACTIVE FILTERS

	Supply voltage (V)	Power	3 dB BW	order	Input range (dB)	Normalized P_d ($\times 10^{-12}$ J)	Ref.
1	1.0	$10.5 \mu\text{W}$	100 kHz	5	68 (max.) 57 (min.)	21.0 21.0	[14]
2	2.5	$40 \mu\text{W}$	70 kHz	2	75	285.7	[15]
3	1.2	$65 \mu\text{W}^q$ $170 \mu\text{W}^m$	320 kHz	3	65	67.7^q 177.1^m	[4]
4	1.5	$375 \mu\text{W}$	525 kHz	5	67	142.9	[16]
5	1.2	6.5mW^q	30 MHz	3	62.5	72.2	[5]
6	1.2	$23 \mu\text{W}$	320 kHz	3	57	24.0	[17]
7	2.5	13 mW	600 kHz	7	77^x 71^x	3095.0 3095.0	[18]
8	1.2	6.5mW^q	100 MHz	3	50	21.7	[5]
9	5	$580 \mu\text{W}$	40 MHz	2	41.3	7.25	[19]
10	2.5	21.6mW^m	930 kHz	3	112	9350	This work

^q In quiescent condition.

^m With the maximum input signal.

^x [18] quotes a maximum signal of $2V_{pp}$, a noise floor of $196 \mu V_{rms}$, and a dynamic range of 77 dB.

These numbers are inconsistent. The value corresponding to the quoted maximum signal and noise is 71 dB.

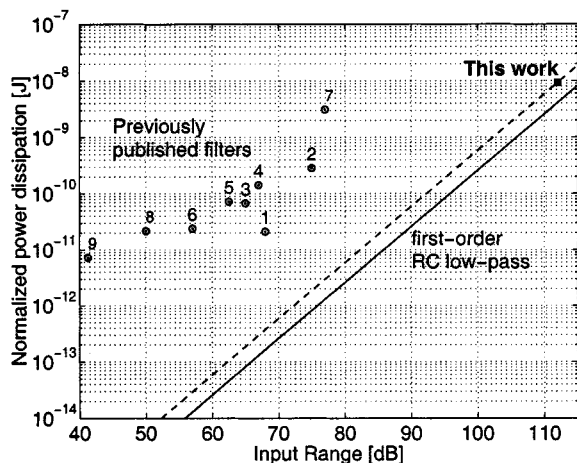


Fig. 18. Comparison of input range and power consumption.

V. CONCLUSION

It is demonstrated that by using adjustable biasing, the power dissipation and output noise of a continuous-time filter can be reduced for small inputs. In the proposed realization of a dynamically biased filter, the linearity and time invariance are preserved during bias transients. An input range of 112 dB is realized in a dynamically biased log-domain filter prototype fabricated in a $0.25\text{-}\mu\text{m}$ BiCMOS technology. Dynamic biasing also enables a quiescent power dissipation that is 40 times smaller than that required to process the largest signal. The results represent over an order of magnitude of improvement in the power efficiency of continuous-time analog filters.

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