A 5Gb/s NRZ Transceiver with Adaptive Equalization for Backplane Transmission

Nagendra Krishnapura
Majid Barazande-Pour
Qasim Chaudhry
John Khoury
Kadaba Lakshmikumar
Akshay Aggarwal

Vitesse Semiconductor, Somerset, NJ
Outline

- Motivation
- Backplane characteristics and equalization
- Architecture of the chip
- Receiver
- Transmitter
- Clock multiplier unit
- Experimental results
- Conclusions
Motivation
Backplane characteristics

- Attenuation from the trace
- Reflection from vias and connectors
- Crosstalk from connectors
⇒ Need equalization
Equalization techniques

- **Transmitter pre-emphasis**
  + Improves eye opening
  - Increases crosstalk

- **Receiver feedforward equalization**
  + Improves eye opening
  - Amplifies crosstalk

- **Receiver decision feedback feedback equalization**
  + Improves eye opening
  + Doesn’t increase crosstalk
  - Can only cancel post cursor ISI
  - Can result in error propagation
Backplane transceiver chip

- 8B/10B in XAUI stripped in the digital core
- 2x XAUI ≡ 5.15Gb/s
- FEC: 3.5dB coding gain
Receiver architecture

- FFE
- VGA
- CDR
- Decision
- 1:16 DEMUX
- FIR
- LMS

Inputs:
- 5Gb/s

Outputs:
- 312.5Mb/s

Feedbacks:
- dc offset
- decision feedback
- coefficients

Clocks:
- $f_s$
- $f_s/16$
FFE

dc path

ac path

\[ \Sigma \]

\[ \text{in} \quad \rightarrow \quad \text{out} \]

\[ C_{FFE} \]

\[ \text{HV}_{dd} \]

\[ V_{dd} \]

\[ l_0 + \Delta l \quad l_0 - \Delta l \]
VGA

\[ \text{in} \rightarrow \pm \Sigma \rightarrow \text{out} \]

\[ \text{c}_{\text{VGA}} \]

\[ \text{HV}_{dd} \]

\[ \text{V}_{dd} \]

\[ \pm l_{1} \pm l_{0} + \Delta l \pm l_{0} - \Delta l \]
Decision feedback equalizer
High voltage bias generator

Voltage doubler

Doubler waveforms:
\[ c_{k}[n+1] = c_{k}[n] - \mu \text{sgn}(e[n]) \text{sgn}(\frac{de[n]}{dc_{k}}) \]
Clock and data recovery
Transmitter

\[ y[n] = c_{-1} x[n-1] + c_0 x[n] + c_1 x[n+1] \]
Clock multiplier unit
Quad 5Gb/s transceiver

- 0.13μm CMOS, 8 metal layers
30” Backplane response

-9.9dB down at half data rate

- Completely closed eye at 5Gb/s
Equalized receiver sensitivity

- Data through 30" FR4 backplane to Rx
- No pre-emphasis or FEC
Transmit pre-emphasis

- Tx Data through 30” FR4 backplane
- Pre-emphasis partially opens the eye
Quad transceiver test setup

- 5.15 Gb/s operation, no FEC
- 30” FR4 backplane, 15m CX4 cable
Quad transceiver performance

- 5.15Gb/s operation, no FEC
- BER < $10^{-15}$ with 30” backplane
- BER < $10^{-15}$ with 15m CX4 cable
## Performance summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.13μm CMOS</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.2V</td>
</tr>
<tr>
<td>Data rate</td>
<td>5.15Gb/s</td>
</tr>
<tr>
<td>Power dissipation (4 channels)</td>
<td>2.1W</td>
</tr>
<tr>
<td>Chip area, including pads</td>
<td>12 sq. mm</td>
</tr>
<tr>
<td>CMU jitter</td>
<td>1.6ps rms</td>
</tr>
<tr>
<td>(Tx o/p with a 1010... pattern, Receivers active)</td>
<td></td>
</tr>
<tr>
<td>Tx total jitter (PRBS31 output)</td>
<td>4.0ps rms</td>
</tr>
<tr>
<td>Tx output (programmable)</td>
<td>200-800mV ppd</td>
</tr>
<tr>
<td>BER(36” backplane trace + test board connections)</td>
<td>&lt; 1e-15</td>
</tr>
<tr>
<td>BER (15m CX4 cable + test board connections)</td>
<td>&lt; 1e-15</td>
</tr>
<tr>
<td>Rx adaptation time</td>
<td>~ 200ms</td>
</tr>
</tbody>
</table>
Conclusions

- A combination of pre-emphasis, FFE, and DFE can equalize a variety of channels.
- The proposed chip enables doubling of data rate over existing channels.
- Transmit and receive equalization and FEC can be used individually or in combination for error free transmission in different settings.
Acknowledgments

- Carlos Carvalho, Jose Matos, and Ruben Recinos for layout.