E6316: Analog systems in VLSI, Fall 2004

HW4 Solutions: Nagendra Krishnapura

1. (a) m^{th} transition of A/D 1 when

$$V_{in} + V_{es/H} = V_{e,AD1}[m] + m V_{LSB}$$

$$V_{in} = V_{e,AD_1}[m] + m V_{LSB} - V_{es/H}$$

(b) D/A output $= m \cdot V_{LSB1} + V_{e,D/A}[m]$

k^{th} transition of A/D 2 when

$$\left[V_{in} + V_{es/H} - \left(m V_{LSB_1} + V_{e,D/A}[m]\right)\right] G + V_{e,amp} = k V_{LSB_2} + V_{eAD_2}[k]$$

$$V_{in} = m V_{LSB_1} + \frac{k V_{LSB_2}}{G} + V_{eD/A}[m] - V_{es/H} - \frac{V_{e,amp}}{G} + \frac{V_{eAD_2}[k]}{G}$$

(c) From (a): $V_{in} = m V_{LSB} + V_{eAD_1}[m] - V_{es/H}$

$$\therefore \left|V_{eA/D_1}[m]\right| + \left|V_{es/H}\right| \leq \frac{V_{LSB}}{2} = \frac{V_{ref}}{2^{M+k+1}} = \frac{V_{ref}}{2^{N+1}}$$

Equal contributions:

$$\left|V_{eAD_1}[m]\right| \leq \frac{V_{ref}}{2^{N+2}} \; ; \left|V_{es/H}\right| \leq \frac{V_{ref}}{2^{N+2}}$$

(d) From (b):

$$\text{Error} = \left|V_{eD/A}[m]\right| + \left|V_{es/H}\right| + \left|\frac{V_{eamp}}{G}\right| + \left|\frac{V_{eAD_2}[k]}{G}\right| \leq \frac{V_{ref}}{2^{N+1}}$$

Equal contributions:

$$|V_{e_{D/A}}[n]| \le \frac{1}{4}\cdot\frac{V_{ref}}{2^{N+1}} = \frac{V_{ref}}{2^{N+3}} \quad \left[\begin{matrix}N+2 \text{ bit}\\ \text{accuracy}\end{matrix}\right]$$

$$* \quad |V_{e_{S/H}}| \le \frac{1}{4}\,\frac{V_{ref}}{2^{N+1}} = \frac{V_{ref}}{2^{N+3}} \quad \left[\begin{matrix}N+2 \text{ bit}\\ \text{accuracy}\end{matrix}\right]$$

$$\left|\frac{V_{e_{amp}}}{G}\right| \le \frac{1}{4}\,\frac{V_{ref}}{2^{N+1}} \;\therefore\; |V_{e,amp}| \le \frac{2^M V_{ref}}{2^{N+3}}$$

$$\{G = 2^M\} \qquad = \frac{V_{ref}}{2^{K+3}}$$

$$\left|\frac{V_{e_{A/D_2}}[k]}{G}\right| \le \frac{1}{4}\,\frac{V_{ref}}{2^{N+1}} \;\therefore\; |V_{e_{A/D_2}}[k]| \le \frac{V_{ref}}{2^{K+3}}$$

stricter condition than in (a)

$k+2$ bit accuracy.

(c) $M=5$, $K=3$

A/D #1: $N+1$ bit accuracy = 9 bit accuracy

S/H : $N+2$ bit accuracy = 10 bit accuracy

D/A : " = 10 bit accuracy

~~D~~amp amplifier : $k+2$ bit accuracy = 5 bit accuracy

A/D_2 : $k+2$ bit accuracy = 5 bit accuracy

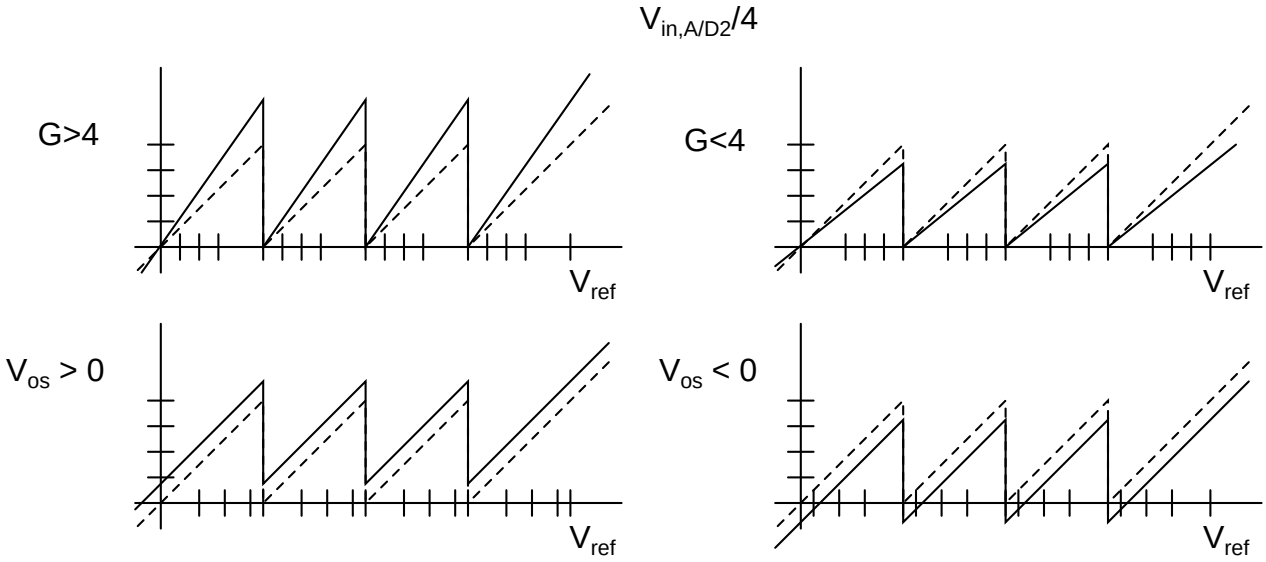
Similarly for $M=4$, $K=4$

A/D #1: 9 bits, S/H & D/A : 10 bits

amplifier and A/D #2 : 6 bits.

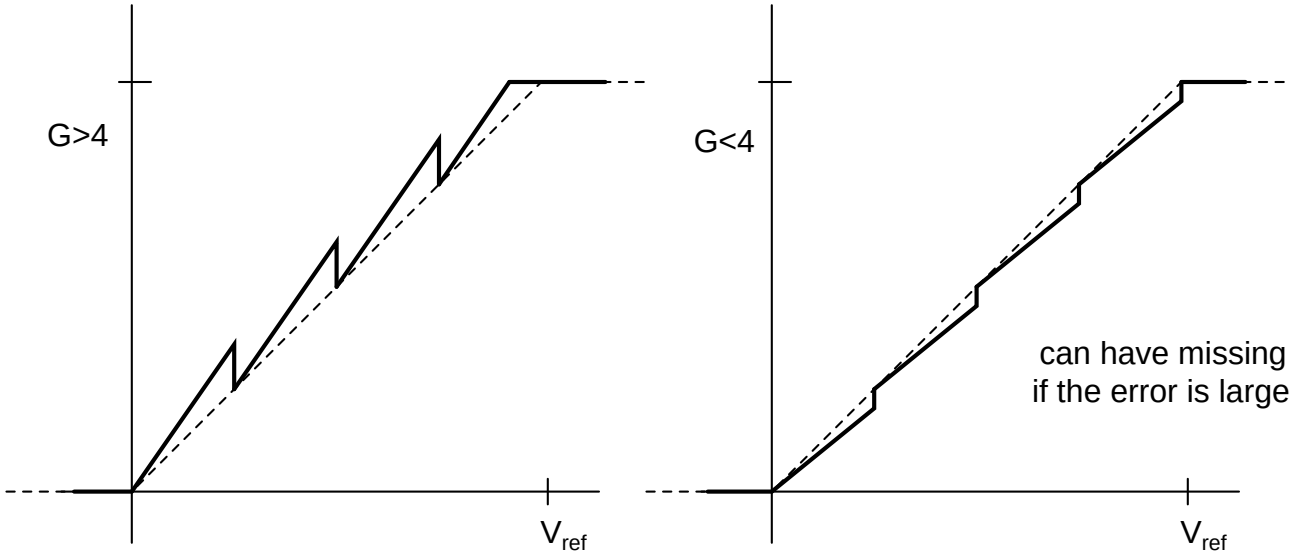
Problem #2: The 2nd A/D quantizes the amplified residue

$V_{in,A/D2}$: The input to the second A/D converter



dashed: ideal, solid: actual

X axis markings show the decision levels.



A/D characteristics shown as a transfer curve(straight line passing through the steps)

They can be similarly generated for the case with offsets