E4316: Analog systems in VLSI

HW3 solutions Nagendra Krishnapura

1) (12.7) Worst case DNL occurs @ MSB transition

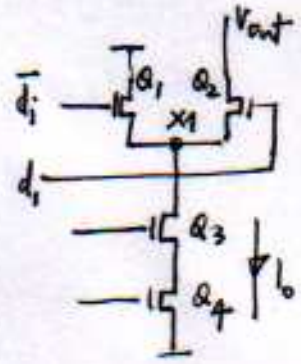
	Ideal	Actual
0 111 1111	127C	$127C(1-0.005) = 126.365$
1 000 0000	128C	$128C(1+0.005) = 128.64$
step	C	2.275C

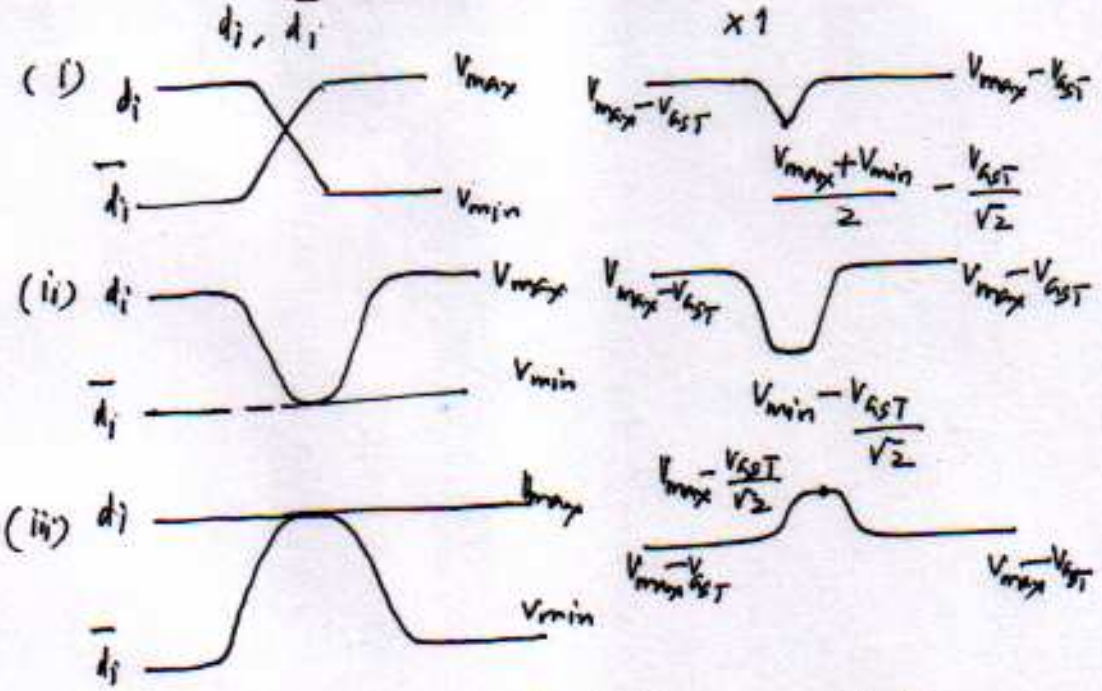
$$DNL = \frac{2.275C - C}{C} = 1.275\,LSB.$$

(12.8)

Define $V_{GST} = V_{GS}(Q_1) - V_T$ when $I_D(Q_1) = I_0$

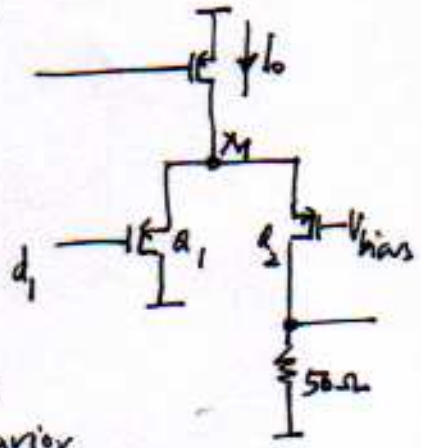
(also $= V_{GS}(Q_2) - V_T$ when $I_D(Q_2) = I_0$)





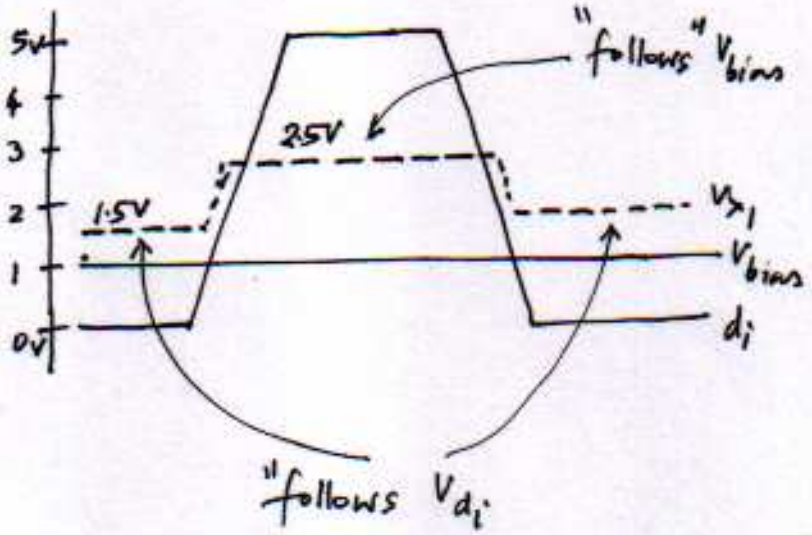
The jump in X1 increases if $d_i, \bar{d}_i$ don't cross at the midpoint of V_{max}, V_{min}

(12.16)



The problem says "threshold voltage", but the gate-source drop is $|V_{GS}| = V_T + (\quad)$.

Assume that $V_{GS}(Q_1) = -1.5V$ @ $I_{DS}(Q_1) = -I_o$

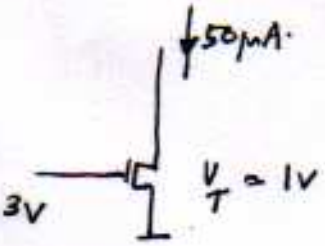


approx. behavior

$V_{d_1} < V_{bias}$: Q_1 acts as a source follower

$V_{d_1} > V_{bias}$: Q_2 acts as a source follower.

(12.18)



$$50\mu A = \frac{92\cdot\mu A/V^2}{2}\cdot\frac{W}{L}\quad(3V-1V)^2$$

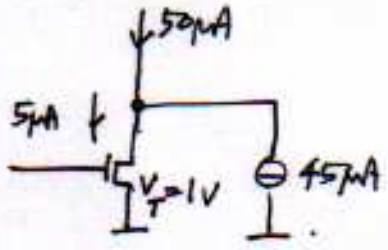
$$\therefore\quad \frac{W}{L} = 0.272$$

$$g_m = 92\mu A/V^2\cdot\frac{W}{L}\quad(3V-1V) = 50\mu S$$

$$\Delta V = 1mV \Rightarrow \Delta I = 50nA$$

$$\frac{\Delta I}{I} = \frac{50nA}{50\mu A} = 0.1\%$$

(12.17)



$$5\mu A = \frac{92\mu A/V^2}{2}\quad\frac{W}{L}\quad(3V-1V)^2$$

$$\therefore\quad \frac{W}{L} = 0.0272$$

$$g_m = 92\mu A/V^2\quad\frac{W}{L}\quad(3V-1V) = 5\mu S$$

$$\Delta V = 1mV \Rightarrow \Delta I = 5nA$$

$$\frac{\Delta I}{I} = \frac{5nA}{5\mu A} = 0.1\%.\quad \frac{\Delta I}{I_{ref}} = 0.01\%$$

12.17, 12.18 :

$$\frac{\Delta I}{I_0} = \frac{g_m \cdot \Delta V}{I_0}$$

$$= \frac{\mu C_{ox} \frac{W}{L} \cdot (V_{GS} - V_T)}{\frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2} \cdot \Delta V \cdot$$

∴ % change in the transistor current is a function of only $(V_{GS} - V_T)$. It is the same for the 2 cases.

2). (a). 10 bit dac.

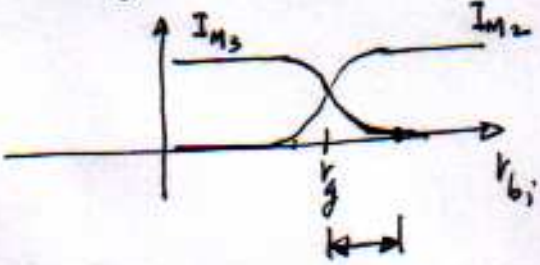
$$I_{unit} = \frac{\Delta V_{out,max}/R}{2^N - 1} = \frac{1.023V/200\Omega}{1023} = 5\mu A$$

(b) $V_{out,min} = V_{dd} - 1.023V = 1.477V$

$V_g - V_{out,min} \leq V_T$ to keep M_3 in saturation

∴ $V_g \leq 2.227V$

(c)



When M_2 just turns off,

$V_{bi} = V_L$

$V_{GS,M_2} = V_T$; $V_{GS,M_3} = V_T + \sqrt{I_{unit} \frac{2L}{\mu C_{ox} W}}$

$V_{bi} - V_{GS,M_2} + V_{GS,M_3} = V_g + \sqrt{I_{unit} \frac{2L}{\mu C_{ox} W}}$

∴ $V_{bi} = V_g - \sqrt{I_{unit} \frac{2L}{\mu C_{ox} W}}$

$V_L = 2.227V - 0.141V = 2.086V$

~~1.75V~~ ~~2.368V~~

Hy $V_H = 2.227V + 0.141V = 2.368V$

(d). Lowest voltage on M_1 drain when M_2 is OFF

$$V_{d,M_1} = V_g - V_{gs,M_3} = V_g - V_T - \sqrt{I_{unit}\frac{2L}{\mu C_{ox} W}}$$

$$= 1.336V$$

$$V_{bias} - V_{d,M_1} \geq V_T$$

$$\therefore V_{bias} \leq 2.086V$$

(e) $\frac{W}{L} = 0.056$

(f) current mismatch between 2 current sources $= \Delta V_T \cdot g_m = DNL \cdot I_{unit}$

$$g_m = \mu C_{ox}\frac{W}{L}(V_{gs}-V_T) = 7.49\mu S$$

~~$g_m \cdot \Delta V_T \leq \frac{I_{LSB}}{4}$~~ given: $g_m \cdot \sigma_{V_T} \leq \frac{I_{LSB}}{4} = 1.25\mu A$

$$\sigma_{V_T} \leq \frac{1.25\mu A}{7.49\mu S} = 167mV$$

INL can be computed, but at the 10 bit level, the ~~desired~~ allowable mismatch is so large that it makes no sense for the DNL specification.

(gate area $\cong 0.101\mu^2$).

If INL is required to be $\leq \frac{1}{4}$ LSB,

$$INL[n] \simeq \frac{n}{N}\sqrt{N-n}\cdot\frac{\sigma(\Delta I)/\sqrt{2}}{I_{unit}}$$

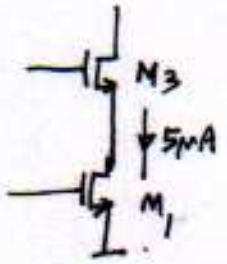
$$INL_{max} \text{ (at } n=N/2) = \frac{1}{2}\sqrt{\frac{N}{2}}\cdot\frac{\sigma(\Delta I)/\sqrt{2}}{I_{unit}} \leq \frac{1}{4}\text{ LSB}$$

$$\sigma(\Delta I) = 0.156\mu A$$

$$\sigma_{V_T} \leq \frac{0.156\mu A}{7.49\mu S} = 20.8mV$$

$WL = 0.058\,\mu m^2$, still very small.

(g)



Assuming 0.5 devices for both M_3 & M_1,

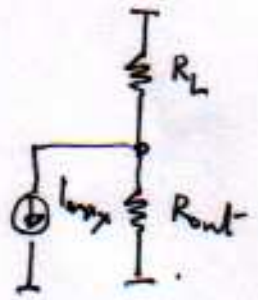
$$\lambda = \frac{0.2V^{-1}}{0.5} = 0.4V^{-1}$$

output resistance $r_{ds} = \frac{1}{\lambda I_d} = 500k\Omega$

$$g_{m_3} = \mu C_{ox}\frac{N}{L}(V_{gs}-V_t) = 70.7\mu S$$

$$r_{out,cell} = g_{m_3} r_{ds_3} r_{ds_1} + r_{ds_1} + r_{ds_3} = 18.7 M\Omega$$

(h). Absolute error of ½ LSB



$$\text{Error} = \left| I_{max}\cdot(R_L \| R_{out}) - I_{max}\cdot R_L \right|$$

$$= I_{max}\cdot\frac{R_L^2}{R_L+R_{out}} = \frac{I_{unit}\cdot R_L}{2} \leftarrow V_{LSB}$$

$$\therefore R_{out} = \frac{2R_L}{I_{unit}/I_{max}} - R_L$$

$$= \left(2\left(2^N-1\right)-1\right)R_L$$

$$\therefore R_{out} = 409k\Omega.$$

$$R_{out} = \frac{R_{out,cell}}{2^N-1} \quad \therefore R_{out,cell} = R_{out}\cdot 2^N - 1$$

(parallel connection) $= 418M\Omega$

[The output resistance computed in (g) is insufficient. A longer channel needs to be used for M_1]

(i) $1fF/\mu m$ capacitance for M_3

$\therefore$ total capacitance $= 2.5\mu m \cdot \frac{1fF}{\mu m} \cdot 1023 = 2.56pF$

Settling to $\frac{1}{2}$ LSB $\left(= \frac{1}{2^{11}}\right)$ ⇒

$$e^{-T_{settle}/\tau} = \frac{1}{2^{11}}$$

$$T_{settle} = \tau \cdot 11 \cdot \ln(2) = RC \cdot 11 \cdot \ln(2) \approx 3.9ns$$

$\therefore$ conversion rate $= \frac{1}{3.9ns} = 256\,MHz$