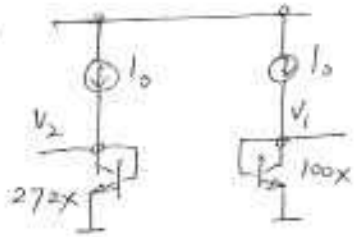
EE316: Analog Systems in VLSI: HW1 Solutions

(Regents's Fellowship)

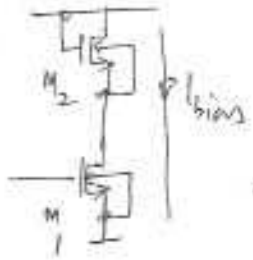
1.



$$V_{out} = V_1 - V_2 = V_t \ln \frac{I_o}{I_s \cdot 100x} - V_t \ln \frac{I_o}{I_s \cdot 272x}$$

$$= V_t \ln\left(\frac{272}{100}\right) \simeq V_t = 26mV$$

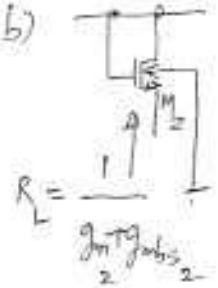
2. (a) Neglect g_{ds}.



$$\frac{V_{out}}{V_i} = -\frac{g_{m1}}{g_{m2}} = -\frac{\sqrt{I_{bias}\mu C_{ox}\frac{W_1}{L_1}}}{\sqrt{I_{bias}\mu C_{ox}\frac{W_2}{L_2}}}$$

$$= -2$$

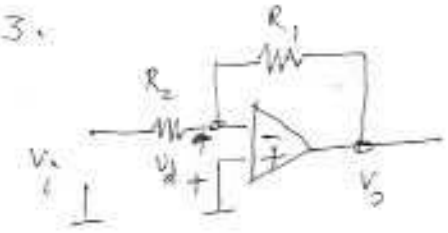
(b)



$$\frac{V_{out}}{V_i} = -\frac{g_{m1}}{g_{m2}+g_{mbs_2}} = -\alpha, \quad \alpha < 2$$

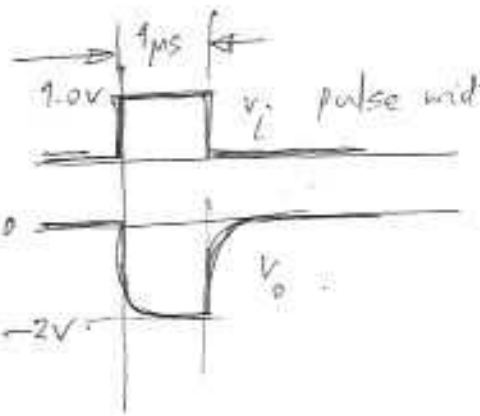
gain reduces

3.



$$\frac{V_o}{V_d} = -\frac{\omega_u}{s}, \quad \omega_u = 2\pi \cdot 3 \cdot 10^6 \text{ rad/s}$$

$$\frac{V_o}{V_i} = -\frac{R_1}{R_2} \cdot \frac{1}{1 + \frac{s}{\omega_u}\cdot\frac{R_1+R_2}{R_2}} = -\frac{2}{1+s\cdot\tau}$$



pulse width $= 2\pi \cdot \tau$

$\tau = \frac{1}{2\pi}\,\mu s$

4 (11.1) $V_{max} = 2^N - 1 \cdot V_{LSB} = 1.023\,V$

(11.2) $V_{LSB} = \frac{V_{ref}}{2^N} = \frac{3V}{2^{12}}$

Quantization noise rms $= \frac{V_{LSB}}{\sqrt{12}}$

Input rms $= \frac{V_{LSB}}{2\sqrt{2}}$

$\therefore$ SNR $= \frac{1/2\sqrt{2}}{\frac{3V}{2^{12}} \cdot \frac{1}{2\sqrt{3}}} = \sqrt{\frac{3}{2}} \cdot \frac{1}{3} \cdot 2^{12} \equiv 64.5dB$

For 0 dB SNR, $V_{i,rms} = \frac{V_{LSB}}{\sqrt{12}} \Rightarrow V_{i,pp} = 2\sqrt{2} \cdot \frac{V_{LSB}}{\sqrt{12}}$

$= \sqrt{\frac{2}{3}} \cdot \frac{3V}{2^{12}} V = 0.6mV$

(11.7) offset error $= V_{out}\Big|_{D_{in}=0} = \frac{-0.01V}{V_{LSB}} = -0.01\,LSB$

$\left[V_{LSB} = \frac{8V}{2^3} = 1V\right]$

Gain $= \frac{7.08 - (-0.01)}{} = 7.09$

Gain error $= 0.09$ $(7.09 - (2^3 - 1))$

Max DNL = [illegible] $= 0.072\,LSB$ See page (3)

Max INL = [illegible] $-0.09\,LSB$ [After gain & offset correction, $V_0'[k] = \frac{V_0[k] + 0.01}{7.09/7.0}$, Compute DNL, INL]

(11.8) Max $^{abs}_{\wedge}$ error $= 0.08V\,(7.08 - 7.0)$

$= 0.08\,LSB \Big|_{3bits} \equiv 6.6$ bits

Max INL $= \log_2 \frac{2^3 \cdot 1\,LSB}{0.09\,LSB} = 6.47$ bits.

$\left[N_{bits} = \log_2 \frac{V_{ref}}{V_{err}} = \log_2 \frac{2^{N,ideal} \cdot V_{LSB,ideal}}{V_{error}}\right]$

(11.10)

	Actual	Ideal
00	0.01V	0V
01	1.02V	1V
10	1.97V	2V
11	3.02V	3V

$V_{LSB} = 1V$

$\text{offset} = \frac{0.01V}{1V} = 0.01\,LSB$

$\text{Gain} = \frac{3.02V - 0.01V}{1V \cdot (2^2 - 1)} = 3.01$

$\text{Gain error} = 3.01 - 3 = 0.01\,LSB$

Worst case absolute error $= -0.02V \cong -0.03LSB$

(11.12) For ΔV (due to jitter) to be less than $1V_{LSB}$,

$$\Delta t < \frac{1}{2^N \pi f_{in,max}} = 2.43 \times 10^{-10} s = 243ps$$

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characteristics of the D/A converter in 11.7

given : -0.01 (*), 1.03, 2.02, 2.96, 3.95, 5.02, 6, 7.08 (**) (*: offset)

remove offset (+0.01) : 0, 1.04, 2.03, 2.97, 3.96, 5.03, 6.01, 7.09 (†) (†: gain)

(** : max. absolute error)

remove gain error ($\times \frac{7.0}{7.09}$) : 0, 1.027, 2.004, 2.932, 3.910, 4.966, 5.934, 7.0

INL : 0, 0.027, 0.004, -0.068, 0.090 (††), 0.034, 0.066, 0 (††: max INL)

DNL : — 0.027, -0.023, -0.072 (☆), -0.023, 0.057, -0.032, 0.066

(☆ : Max DNL)