Fall 2004; E6316: Analog Systems in VLSI; HW3

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1. Textbook problems 12.7, 12.15, 12.16, 12.17, 12.18

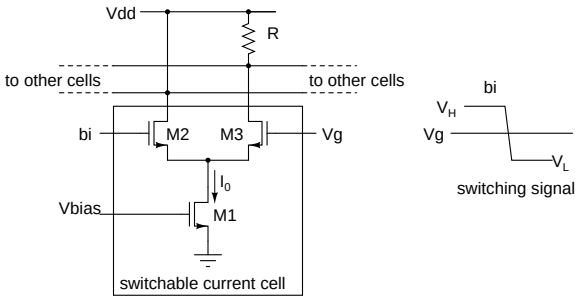

Figure 1:

2. Fig. 1 shows one of the cells of a 10 bit current mode DAC with a full scale output (difference between the maximum and minimum output voltages) of 1.023 V. The output resistance is 200 Ohm. It is being designed in a technology which has $\mu C_{ox} = 100\,\mu\text{A}/V^2$, $V_T = 0.75\,V$, $\lambda = 0.2\,V^{-1}/L$ (where L is in microns), $V_{dd} = 2.5\,\text{V}$

   (a) What is the tail current of the unit cell?

   (b) What is the largest possible V_g?

   (c) For the above V_g, what are the values of V_H and V_L required to turn on and off the differential pair M_2, M_3? M_2, M_3 have $W/L = 2.5\,\mu\text{m}/0.5\,\mu\text{m}$

   (d) What is the lowest voltage at the drain of the current source transistor $M1$? What is the largest possible gate bias V_{bias}?

   (e) For this gate bias, compute W/L for the current source transistor.

   (f) Assuming that threshold voltage variations are the only source of mismatch, compute the gate area of the current source device to obtain a DNL standard deviation (σ) of 1/4 LSB. Compute W and L. (use the model $\sigma_{V_T} = A_{V_T}/\sqrt{WL}$ with $A_{V_T} = 5\,\text{mV}\,\mu\text{m}$)

   (g) What is the output impedance of the unit current cell (when it is on)?

   (h) What is the minimum possible output impedance of the unit cell such that the largest deviation (compared to when each cell is an ideal current source) in the DAC output is 1/2LSB?

(i) Assuming that the settling time is governed by the drain capacitance of M_3, compute the settling time (to 1/2LSB) and the maximum conversion rate of the converter. Assume 1 fF/μm drain capacitance for M_3.