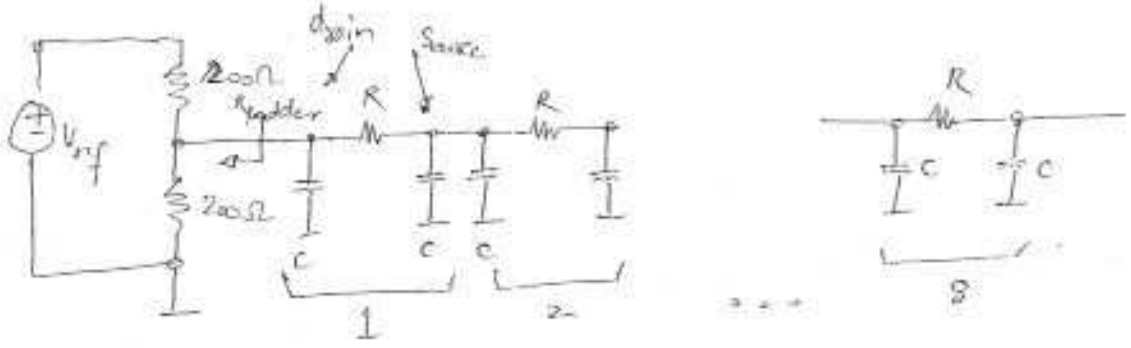
E6316: Analog systems in VLSI : HW2 Solutions

Nagendra Krishnapura

(1) (12.2) Worst case R_{ladder} : code = 1000 0000 (middle tap)



$$\tau_{oc} = R_{ladder} \cdot C + (R_{ladder} + R) \cdot 2C + (R_{ladder} + 2R) \cdot 2C + \dots + (R_{ladder} + 8R) \cdot 2C$$

$$= R_{ladder} \cdot 17C + 2C \cdot R \cdot \frac{8 \cdot 9}{2}$$

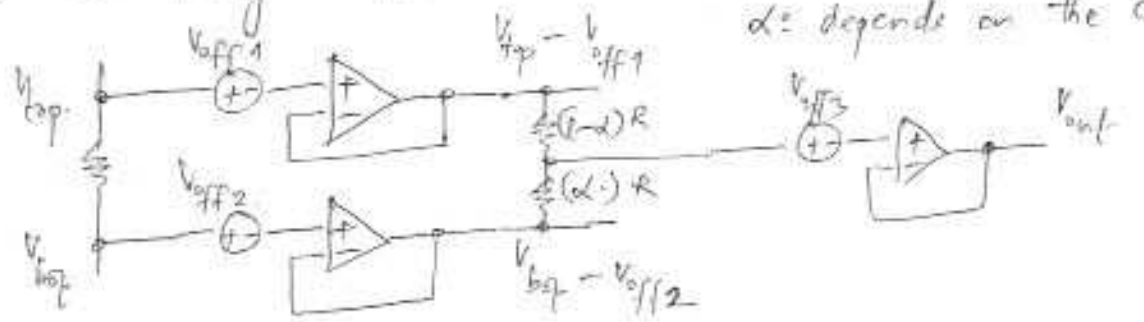
$$= R_{ladder} \cdot 17C + 72RC$$

$$= 3.05\text{ns}$$

~~(X.X.X)~~ Settling time to 0.1% = 6911 τ = 21.1ns

(12.4) 2 string DAC

α: depends on the code $0 \le \alpha \le 1$



$$V_{out} = (V_{top} - V_{off1})(1-\alpha) + (V_{bot} - V_{off2})\alpha + V_{off3}$$

$$= \underbrace{V_{top}(1-\alpha) + V_{bot} \cdot \alpha}_{\text{ideal output}} + \underbrace{\left[-V_{off1}(1-\alpha) - V_{off2} \cdot \alpha - V_{off3} \right]}_{\text{error}}$$

Assuming worst case addition of error and identical offsets, $[V_{off1} = V_{off2} = V_{off3} = V_{off}]$.

$$V_{error} = 2 \cdot V_{off} \leq V_{LSB} = \frac{5V}{2^{10}}$$

$$\therefore V_{off} \leq \frac{5V}{2^{11}} = 2.44\,mV$$

[This is assuming that all 3 opamp offsets are simultaneously present & adding in the worst case. If each is present by itself, $V_{off} \leq \frac{5V}{2^{10}} = 4.88mV$]

(12.6)

$$-V_{out} = \left[\frac{b_1}{2R(1+\alpha_1)} + \frac{b_2}{4R(1+\alpha_2)} + \frac{b_3}{8R(1+\alpha_3)} + \frac{b_4}{16R(1+\alpha_4)}\right] R \cdot V_{ref}$$

$$= \underbrace{\left[\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}\right] V_{ref}}_{\text{ideal output}} + \underbrace{\left[b_1 \cdot \frac{\alpha_1}{2} + b_2 \cdot \frac{\alpha_2}{4} + b_3 \cdot \frac{\alpha_3}{8} + b_4 \cdot \frac{\alpha_4}{16}\right] V_{ref}}_{\text{error.}}$$

Allowable error = $\frac{V_{ref}}{2^{10}}$ (10 bit linearity; but the absolute linearity requirement is irrelevant here. what is asked for is the comparative accuracy requirements of the 4 resistors)

Error due to each resistor = $\epsilon \cdot V_{ref} \left(= \frac{V_{ref}}{2^{10}}\right)$.

$$\frac{\alpha_1}{2} = \frac{\alpha_2}{4} = \frac{\alpha_3}{8} = \frac{\alpha_4}{16} = \epsilon.$$

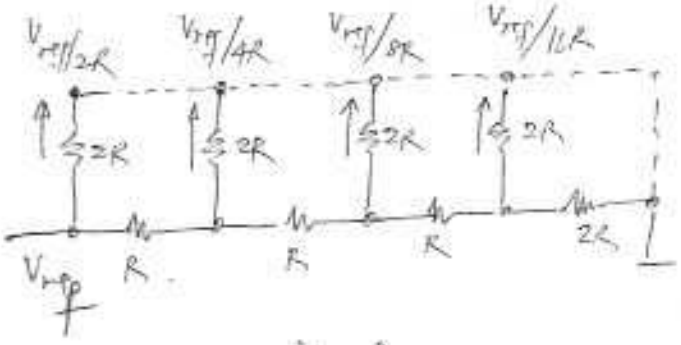
$\alpha_2 = 2\alpha_1$

$\alpha_3 = 4\cdot\alpha_1$

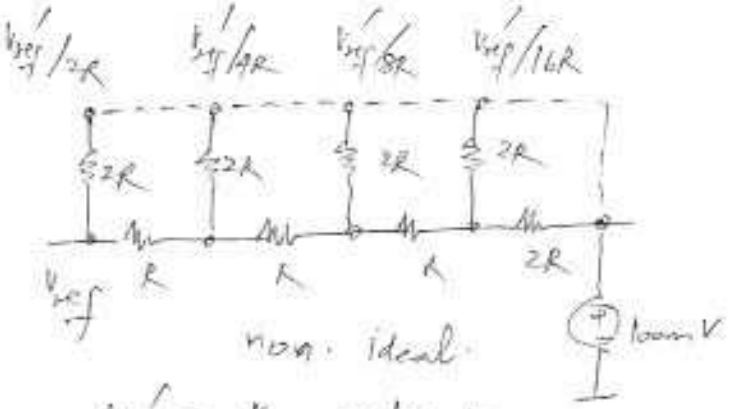
$\alpha_4 = 8\cdot\alpha_1$

} Lower significant bits can be successively worse.

(12.16). The ends of all the '2R' resistances in the circuit are at 100mV instead of 0V in the ideal case.



ideal



non-ideal.

$V'_{ref} = V_{ref} - 100mV$

All the currents are scaled by $\frac{V'_{ref}}{V_{ref}}$.

$\therefore$ D/A output $V_{out} = \frac{V'_{ref}}{V_{ref}}\left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}\right)$

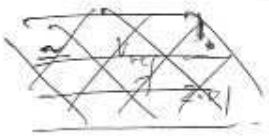
$= (V_{ref} - 100mV)\left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}\right)$

100mV drop across all the switches simply scales the reference voltage. This shows the importance (⇒ switch conductance) of scaling the switch sizes with the currents they carry (so that the voltage remains a constant).

(12.11). $R_A = 2.01 R_B \quad (R_B = R)$

$$-V_{out} = V_{ref} \cdot \left(\frac{b_1}{2.01} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16} \right)$$

$$\text{Error} = \left(V_{ref} \cdot \frac{b_1}{2.01} - V_{ref} \cdot \frac{b_1}{2.0} \right) \quad (b_1 = 1)$$



$$\simeq -V_{ref} \frac{1}{2} (0.005)$$

$$\text{Error (in LSB)} = 0.04 \text{ LSB} \qquad V_{LSB} = \frac{V_{ref}}{2^4}$$

(Fig. 1)

2 (a). $V_{out}\Big|_{D_{in}=0} = V_{os}$

$$V_{out}\Big|_{\substack{D_{in}=15\\(1111)}} = V_{os}\left(1+\frac{R_f}{R_1}\right) + \underbrace{V_{ref}\cdot\frac{15}{16}}_{\text{ideal output}}$$

$$= V_{os}\left(1+\frac{15}{16}\right) + V_{ref}\cdot\frac{15}{16}$$

$$\text{Gain} = \frac{V_{ref}\cdot 15/16 + V_{os}\cdot 15/16}{V_{ref}/16} = 15 + \frac{V_{os}}{V_{ref}}\cdot 15 = 15\left(1+\frac{V_{os}}{V_{ref}}\right)$$

$\therefore$ offset, after adjusting (Grading) for gain error

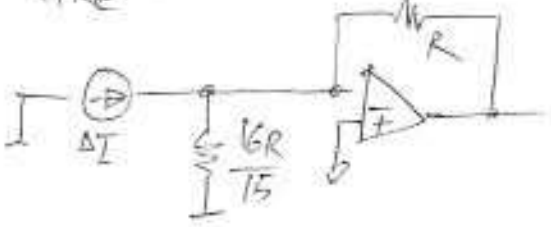
$$= \frac{V_{os}}{\left(1+\frac{V_{os}}{V_{ref}}\right)}\cdot\frac{1}{V_{ref}/16} = 16\cdot\frac{V_{os}/V_{ref}}{1+V_{os}/V_{ref}} \quad (\text{in LSBs})$$

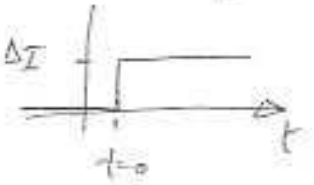
(b) For offset = 1LSB; $\dfrac{V_{os}}{V_{ref}} = \dfrac{1}{15}$

input bits.

(c) Lowest bandwidth when all ~~xxxxxxx~~ are on (= 1)

when the code switches to 1111, the picture looks like





ΔI is the difference between the current being fed to the virtual ground between the current & previous code.

$$-V_{out} = \frac{\Delta I(s) \cdot R}{1 + \frac{s}{\omega_n} \cdot \frac{R + R/15}{16/15 R}} = \frac{\Delta I(s) \cdot R}{1 + \frac{s}{\omega_n} \cdot \frac{31}{15}}$$

settling time constant $= \frac{31}{15\omega_n}$

For settling to $\frac{1}{4}$ LSB $\left(\frac{1}{2^6}\right)$, # time constants $= 4.2$

$$4.2 \cdot \frac{31}{15 \cdot \omega_n} = 100\text{ns}$$

$$\omega_n = 13.7\text{MHz} \cdot 2\pi = 86\ \text{Mrad/s}$$

Fig. 2

(a). $+V_{out}\Big|_{D_{in}=0} = V_{os}$

$$V_{out}\Big|_{D_{in}=k} = -V_{ref} \cdot \frac{k}{16} + V_{os}\left(1 + R \cdot G_{in}[k]\right)$$

$G_{in}[k]$: ~~xxxxxxxx~~ impedance looking in to the ladder from the virtual ground.

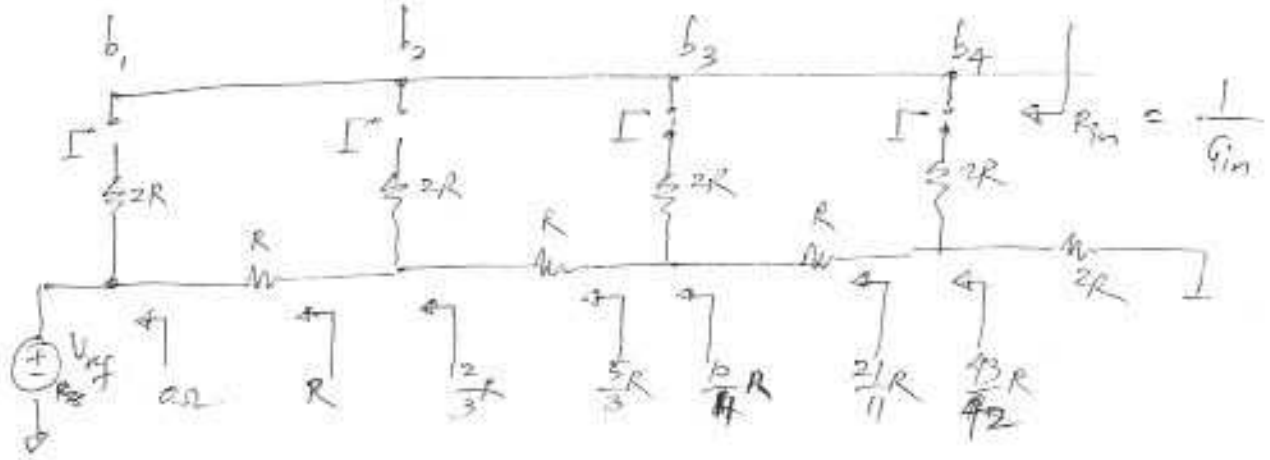
[see next page for detailed calculations]

$$V_{out}\Big|_{D_{in}=15} = -\frac{15}{16} V_{ref} + 2.5495 \cdot V_{os}$$

$$\text{DAC gain} = \frac{V_{out}\Big|_{D_{in}=15} - V_{out}\Big|_0}{V_{LSB}} = -15 + (1.5495) \cdot 16 \cdot \frac{V_{os}}{V_{ref}}$$

$$DNL[k] = \frac{1}{-V_{LSB}} \cdot \frac{V_{out}[k] - V_{out}[k-1]}{\text{Gain}/\text{ideal gain}} - 1$$

$$= \frac{1}{V_{LSB}} \cdot \frac{V_{LSB} - V_{os} \cdot R\left(G_{in}[k] - G_{in}[k-1]\right)}{\text{Gain}/\text{ideal gain}} - 1.$$



$b_1 = 1,\ b_2 = b_3 = b_4 = 0$; $R_{in_1} = 2R$

$b_2 = 1,\ b_1 = b_3 = b_4 = 0$; $R_{in_2} = \frac{8}{3}R$

$b_3 = 1,\ b_1 = b_2 = b_4 = 0$; $R_{in_3} = \frac{32}{11}R$

$b_4 = 1,\ b_1 = b_2 = b_3 = 0$; $R_{in_4} = \frac{127}{42}R$

$$\frac{1}{R_{in}} = \frac{b_1}{2R} + b_2 \cdot \frac{3}{8R} + b_3 \cdot \frac{11}{32R} + b_4 \cdot \frac{42}{127R}$$

b_4 increment : $\Delta G_{in} = \frac{42}{127R} = \frac{0.3307}{R}$ $\left(\frac{1}{R_{in_4}}\right)$

b_3 increment : $\Delta G_{in} = 0.0130/R$ $\left(\frac{1}{R_{in_3}} - \frac{1}{R_{in_4}}\right)$

b_2 increment : $\Delta G_{in} = -\frac{0.2995}{R}$ $\left(\frac{1}{R_{in_2}} - \frac{1}{R_{in_3}} - \frac{1}{R_{in_4}}\right)$

b_1 increment : $\Delta G_{in} = -\frac{0.5495}{R}$

when $b_1 = b_2 = b_3 = b_4 = 1$, $G_{in} = 1.5495/R$

$$V_{out} = -\frac{15}{16} \cdot V_{ref} + 2.5495 \cdot V_{os}$$

CALCULATING R_{in}

For simplicity of expression, ignore gain error.

$$DNL[k] = -\frac{V_{os}}{V_{LSB}} R\left(G_{in}[k] - G_{in}[k-1]\right)$$

Largest $G_{in}[k]$ occurs when MSB (b_1) turns on

$$G_{in}[k] - G_{in}[k-1] = \frac{0.5495}{R} \cdot$$

$$\left(= G_{in_1} - G_{in_2} - G_{in_3} - G_{in_4}\right)$$

$$DNL\Big|_{max} = \frac{0.5495 \cdot V_{os}}{V_{LSB}} \cdot$$

with gain error,

$$DNL_{max} = \frac{0.5495\, V_{os}/V_{LSB}}{1 + \frac{15}{15}(2.5495)\frac{V_{os}}{V_{ref}}}$$

(b) For $DNL_{max} = 1 LSB$, $V_{os} = \frac{V_{LSB}}{0.5495}$.

(c). Lowest bandwidth when all bits turned on.

$$G_{in} = G_{in_1} + G_{in_2} + G_{in_3} + G_{in_4} = \frac{1.5495}{R}.$$

$$\text{Bandwidth} = \frac{\omega_u}{1 + R \cdot \frac{1.5495}{R}} = \frac{\omega_u}{2.5495} \quad (\text{rad/s})$$

time constant, $\tau = \frac{2.5495}{\omega_u}$

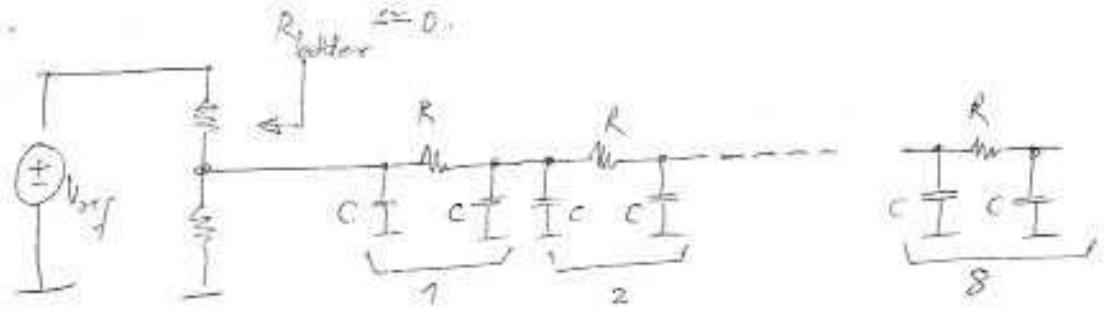
$$4.2\tau = 4.2\,\frac{2.5495}{\omega_u} = 100\,ns$$

$$\omega_u = 107\ \text{Mrad/s} \quad (= 17.05\ \text{MHz}).$$

(3) (a) $R_{mos} = \frac{L}{W \cdot \mu C_{ox}} \cdot \frac{1}{V_{GS} - V_T}$

Use $L = 0.25\mu m$, the minimum available. This results in the lowest resistance for a given bias & width.

(b)



$\tau = 2C \cdot R + 2C \cdot 2R + \cdots + 2C \cdot 7R + C \cdot 8R$

$= 2C \cdot \frac{8 \cdot 9}{2} - C \cdot 8R = \underline{64RC}$

$t_{settling}\Big|_{\frac{1}{4}LSB = \frac{1}{2^{12}}} = 8.3\tau = \underline{532.3RC}$

$R = \frac{L}{W \cdot \mu C_{ox}} \cdot \frac{1}{V_{GS} - V_T}$; $C = W \cdot C_W$ $\boxed{C_W = 1fF/\mu m}$

$\therefore t_{settling} = 532.3RC = 532.3 \frac{L \cdot C_W}{\mu C_{ox}(V_{GS} - V_T)}$

$L = 0.25\mu m$; $C_W = 1fF/\mu m$; $\mu C_{ox} = 100\mu A/V^2$; $(V_{GS} - V_T)_{min}$

Minimum bias $(V_{GS} - V_T)$ when the top of the R-string is connected to the output

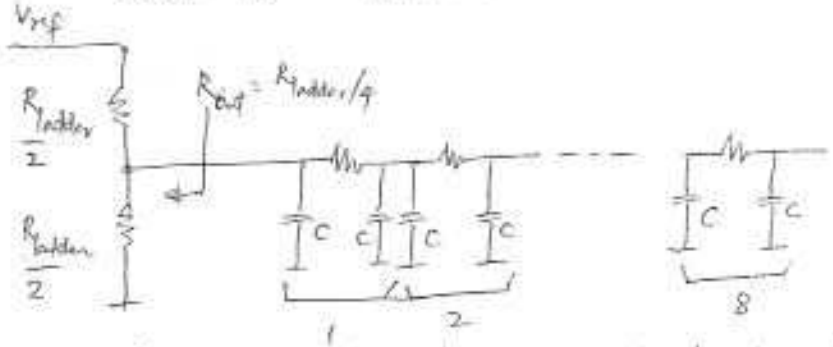
$= (2.5V - 1V - 0.75V)$

$= 0.75V$

$\therefore t_{settling} = 1.77ns$

Conversion rate $= \frac{1}{1.77ns} = 564MHz$

© Worst case ladder resistance when the middle code is selected.



Open circuit time constant due to the ladder

$= R_{out} \cdot 16C$

$R_{out} \cdot 16C = 64 \cdot RC$

$\frac{R_{ladder}}{4} = R_{out} = 4 \cdot R$

$\therefore R_{ladder} = 16 \cdot R$

$I_{ladder} = \frac{V_{ref}}{R_{ladder}}$

Absolute values can be calculated only if the switch width is known.

For $W = 2\mu m$,

$R = 1.67 k\Omega$

$R_{ladder} = 26.7 k\Omega$

$I_{ladder} = 37.5 \mu A$

(d) opamp unity gain frequency $= \omega_u$

Settling time constant due to the opamp $= \frac{1}{\omega_u}$

$8.3 \frac{1}{\omega_u} = t_{settling,switch} = 1.77ns$

$\omega_u = 4.7 Grad/s$; opamp unity gain frequency

$f_u = 746 MHz$.

(e) When all three are present,

~~net transfer function~~

net settling time $\simeq t_{settling,1} + t_{settling,2} + t_{settling,3}$

$= 3\ (1.77\ ns) = 5.31\ ns$

Conversion rate $= \frac{1}{5.31\ ns} = 188\ MHz.$