Fall 2004; E6316: Analog Systems in VLSI; HW2

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1. Textbook problems 12.2, 12.4, 12.6, 12.10, 12.11, 12.14

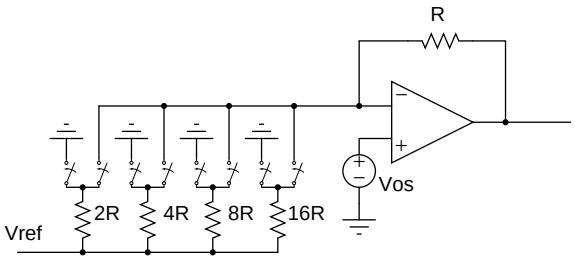

Figure 1:

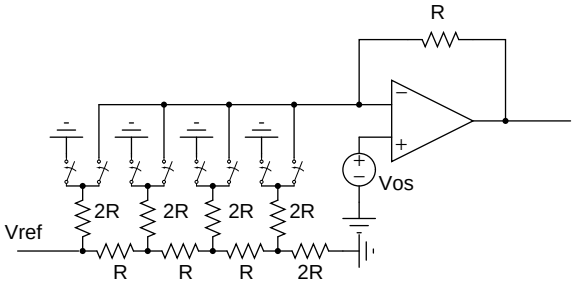

Figure 2:

2. In Fig. 1 and Fig. 2 compute

   (a) The offset voltage of the DAC in terms of the opamp offset Vos

   (b) The maximum Vos such that the maximum DNL is smaller than 1 LSB.

   (c) The unity gain frequency of the opamp such that the output can settle to $1/4$ LSB in 100ns.

3. **Design of an 8 bit resistor string D/A converter (Fig. 12.1 in the text) with $V_{ref} = 1$ V and a supply voltage $V_{dd} = 2.5$ V**: Use single channel MOS switches. You have MOS transistors with $\mu C_{ox} = 100\,\mu\text{A}/V^2$, $V_T = 0.75\,V$. Assume that the MOS transistors have 1 fF of drain/source parasitic capacitance per micron width (W).

(a) The minimum MOS transistor length(L) in the technology is $0.25\,\mu$m. What length would you use for the switches? Why?

(b) Assume that the resistor string has a very small resistance, and that the speed of the D/A converter is limited only by the delay through the switch network. What is the *worst case* settling time? (Consider settling to 1/4 LSB, use the method of open circuit time constants). What is the resulting maximum conversion rate?

(c) Now consider the effects of the resistor string. What is the value of each resistor in the string such that its worst case contribution to the settling time equals that computed above for the switch network. What is the current flowing through the resistor string for this resistance value?

(d) What is the unity gain frequency of the opamp such that its settling time to the desired accuracy (1/4 LSB) equals the settling time computed for the switch network computed in the first part?

(e) In presence of all three of the above contributions to the settling time, approximately compute the conversion rate of the D/A converter.