ABSTRACT

Design Techniques for Low-Noise
LC Voltage-Controlled Oscillators

Babak Soltanian

This dissertation investigates several design techniques to improve performance of LC Voltage-Controlled Oscillators (LC-VCO). First, AM-to-FM noise conversion by MOS device parasitics in differential LC-VCOs is examined and it is shown that there is an optimal oscillation amplitude where this conversion is minimum. The optimum amplitude for lowest AM-to-FM conversion also yields the lowest phase noise for this oscillator. The presented analysis is confirmed with simulation and measurement results for a 2-GHz differential nMOS VCO fabricated in a 0.25-μm BiCMOS process.

Next, a tail-current-shaping technique in LC-VCOs is presented to increase the oscillation amplitude and to reduce the phase noise while keeping the power dissipation constant. In this technique, the tail current is made large when the oscillator output voltage reaches its maximum or minimum value and when the sensitivity of the output phase to injected noise is the smallest; the tail current is made small during the zero crossings of the output voltage when the phase noise sensitivity is large. The operation
and performance of the presented circuit is extensively analyzed and compared to an ideal pulse-biased technique. The presented analysis is confirmed with measurement results of two 2-GHz differential nMOS VCOs fabricated in a 0.25-μm BiCMOS process.

Then, a low-phase-noise quadrature LC-VCO with inherent tail-current shaping is presented. Two identical differential LC-VCOs are locked in quadrature with a capacitor connected between their common-source nodes. This capacitor further drives the oscillators into a tail-current-shaping mode, which increases their oscillation amplitude and reduces their phase noise. The stability of quadrature operation is analyzed and verified. A multi-hand 1.9-GHz differential nMOS quadrature LC-VCO prototype has been fabricated in a 0.25-μm BiCMOS process.

Finally, a fully integrated 0.024-mm² 6-GHz LC-VCO for 6+ Gbps high-speed serial (HSS) links in a 90-nm bulk CMOS is presented. It is comparable in size to ring oscillators, but it has better phase noise. It is less than one fifth the size of any LC-VCO reported to date at this frequency. Using a differential control, a very wide tuning range from 4.5 GHz to 7.1 GHz (45%) is achieved. Additionally, a circuit technique employing a differential inductor’s center tap is presented to dynamically set the differential tune signals’ common mode equal to the VCO’s output common mode.