Body-voltage estimation in digital PD-SOI circuits and its application to static timing analysis

Kenneth L. Shepard and Dae-Jin Kim
Columbia Integrated Systems Lab, Department of Electrical Engineering
Columbia University, New York, NY 10027

Abstract

We describe a technique for estimating the floating body potentials of partially-depleted silicon-on-insulator (PD-SOI) circuits under steady switching activity and under initial activity after a long period of quiescence. The approach is based on a unique state diagram abstraction of the PD-SOI FET that captures all of the essential device physics. This picture yields a simple analytic model of the body voltage which is used within the context of a prototype transistor-level static timing analysis engine. Results are presented that demonstrate the accuracy of the analytic body-voltage model and the reduction in delay uncertainty possible with this technique.

1 Introduction

Silicon-on-insulator (SOI) technology has long found niche applications for radiation-hardened or high-voltage integrated circuits. Recently, SOI has emerged as a technology for high-performance, low-power deep-submicron digital integrated circuits [1, 2]. For digital applications, fully-depleted devices have been largely abandoned in favor of partially-depleted technology because of the difficulty in controlling the threshold voltage of fully-depleted thin-film transistors. Partially-depleted SOI (PD-SOI) has two main advantages for digital applications: the reduction of parasitic source-drain depletion capacitances and the reduction of the reverse-body effect in stack structures and pass-transistor logic.

At the device and circuit level, however, the floating body effect in partially-depleted SOI (PD-SOI) poses "uncertainties" in the body potential, and hence the threshold voltage of a FET, while the parasitic bipolar effect can result in noise failures[5]. Design margining required to offset uncertainties in body voltage can erode potential performance advantages under nominal operation. For circuit styles in which noise margin is strongly determined by threshold voltage (e.g. dynamic circuits), considerable overdesign for noise can also result from conservative body-voltage margining. Previous circuit-level modelling work on PD-SOI has focussed on device issues [3, 4] or delay and noise effects due to the floating-body effect evident for particular circuits under periodic stimulus [5, 6] (pulse stretching, frequency-dependent delay time). In this paper, we present the first techniques to quantify floating-body effects over tens of millions of transistors through static analysis.

We consider characterizing the body-voltage uncertainty of PD-SOI devices using knowledge of switching activity. Each FET of a circuit is analyzed to determine the minimum and maximum possible body voltage (the body-voltage uncertainty) under both "initial-condition" and "steady-state" operation. Initial-condition operation holds for circuits that are quiescent for a long time before undergoing switching activity. Steady-state body-voltage estimation takes into account average switching behavior of the circuit that has been consistently present for a long time. Two techniques are considered for steady-state body-voltage estimation. The first assumes only that the circuit is under reasonably steady switching activity while the second technique, which has less uncertainty, requires knowledge of signal probabilities and arrival times. This body-voltage estimation technique is applied to transistor-level static timing analysis [7], but can be extended to static noise analysis [8] It can also be used in circuit simulation to avoid the need for long simulation runs to establish steady-state body-voltage values.

In this paper, we work with BSIM3SOI [9] models for an IBM partially-depleted SOI technology described elsewhere [10]. Devices have a $0.25\mu m$ effective channel length, $5-nm$ gate oxide, $350-nm$ back oxide, and $140-nm$ thin silicon film. Two supply voltage are considered – 1.0V and 2.5V. While the detailed results presented here apply to this technology, the techniques are generally applicable to any PD-SOI technology.

In Section 2, a state-diagram abstraction of the PD-SOI FET which simplifies the device physics determining the body voltage is presented. In Section 3, a simple analytic model is derived which can be used to accurately predict the body voltages in PD-SOI circuits under both initial-condition and steady-state operation. Section 4 describes a prototype transistor-level static timing analysis engine which incorporates these body voltage characterizations. Some timing analysis results are presented in Section 5. Section 6 concludes and offers direction for future work.

2 State diagram view of body interactions

The body potential of a PD-SOI FET is determined by capacitive coupling of the body to the gate, source, and drain, by diode currents at the source-body and drain-body junctions (including gate-induced drain leakage (GIDL) [11]), and by impact ionization currents produced by current flow through the device (sometimes referred to as the on-state impact ionization current). To model the switching history determining the body voltage of a particular device, we use the state diagram abstraction shown in Figure 1 (for an nFET). The states denoted with solid circles represent "static" states, valid logic conditions for a FET at the end of a cycle. For example, state 1 corresponds to the case in which the gate is high and both the source and drain are low. States 6a and 6b, denoted with dashed circles, are "dynamic" states since for CMOS designs that do not draw dc current, these states will be present only transiently during switching events. Arrows indicate possible state transitions produced by switching events in the circuits containing these FETs. These switching events can represent transitions from the logic state at the end of the previous cycle to the logic state at the end of the current cycle or can represent hazards that occur transiently within a cycle. The states 1, 2, 5a, and 5b are distinguished in Figure 1 with dashed boxes because transitions between these states propagate timing delays. These are also the state in which FETs would be susceptible to noise (glitches). States 5a and 5b can usually be treated equivalently as state 5; similarly states 6a and 6b can be treated equivalently as state 6. The state diagram of the pFET is the "dual" of Figure 1, in which the gate is high rather than low in states 3, 4, and 5; and low rather than high in states 1, 2, and 6.

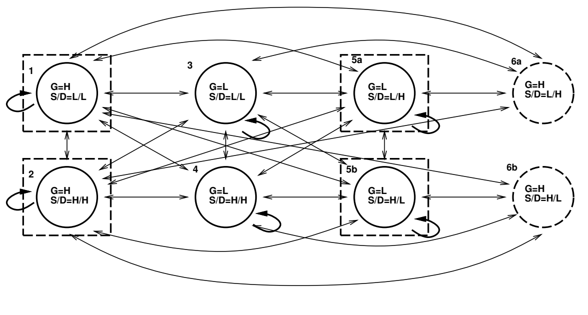

Figure 1: State diagram for a PD-SOI nFET.

In analyzing the device physics determining the body potential, it is convenient to distinguish "slow" and "fast" processes. Fast processes can change the body potential on time scales on the order of or less than the cycle time, while slow processes require time scales much longer than the cycle time (up to milliseconds) to affect the body voltage. There are two fast mechanisms at work: switching transitions on the gate, source, or drain which are capacitively coupled to the body, and forward-bias diode currents across source-body and drain-body junctions with voltages exceeding the diode turn-on voltage. The coupling "kicks" associated with the first mechanism occur for each transition in Figure 1 and are completely reversible on "fast" time scales; that is, if one begins in state 1 and traverses the state diagram, returning to state 1 on a time scale comparable or less than the cycle time, the body voltage on return will be the same as the initial body voltage (a simple statement of charge neutrality). The reversibility of the kicks is, of course, dependent on not triggering the fast irreversible discharge of the body through a forward-biased junction. In practice, this discharge mechanism is only triggered on activation of a circuit after a long period of quiescence. Once the discharge happens (usually within the first few cycles of operation), it is not triggered again as long as the circuit is under steady switching activity. This discharge, when associated with a transition to state 5, can produce parasitic bipolar leakage.

The slow processes involve charging or discharging the body through reverse-biased or very weakly forward-biased diode junctions and through impact ionization. These leakage currents give each state a comparatively slow (much longer than the cycle time) relaxation to a target dc body voltage for each state in Figure 1.

3 Determining the body potential

In this section, we introduce a simple analytic model for the floating body potential of a PD-SOI FET based on the state diagram abstraction of Figure 1. We are implicitly assuming that the digital circuits under consideration are part of a discrete-time system characterized by a cycle (usually defined by the action of a clock) with a cycle time t_{cycle}. This enables us to consider the behavior of the body over a long period of time to be determined by an "average" cycle repeated over and over. Such an average cycle is shown in Figure 2, divided into a series of time slices t_i^{eff}, which characterize the amount of time per cycle on the average that the FET spends in state i. Of course, the time slices sum to the cycle time:

$$\sum_{i=1}^{6} t_i^{eff} = t_{cycle} \tag{1}$$

3.1 Body-voltage model

In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or *displacements*, d_i, (see Figure 2) between the body voltage in state i and the body voltage in the reference state (the *reference body voltage*, which we denote as V_B^{ref}). The particular choice of reference states we have made ensures that all of the d_i are negative for the nFET and positive for the pFET. In addition, each state is relaxing to the target dc values, s_i. The time constants for this relaxation are denoted as τ_i. Except for the fast discharge associated with a source-body or drain-body junction that becomes strongly forward biased, these time constants are much larger than t_{cycle}, and any voltage change during a single time slice would be imperceptible in Figure 2. From this simple picture, one can relate the body voltage at the end of the cycle v_{n+1} to the body voltage at the beginning of the cycle v_n by:

$$v_{n+1} = v_n e^{\sum_{i=1}^{6} -t_i^{eff}/\tau_i} + \sum_{i=1}^{6} (s_i - d_i)(1 - e^{-t_i^{eff}/\tau_i}) e^{\sum_{j=i+1}^{6} t_j^{eff}/\tau_j} \tag{2}$$

The steady-state solution of this difference equation (in the approximation that the τ_i are much greater than t_{cycle}) is given by:

$$V_B^{ref} = \frac{\sum_{i=1}^{6} (t_i^{eff}/\tau_i)(s_i - d_i)}{\sum_{i=1}^{6} t_i^{eff}/\tau_i} \tag{3}$$

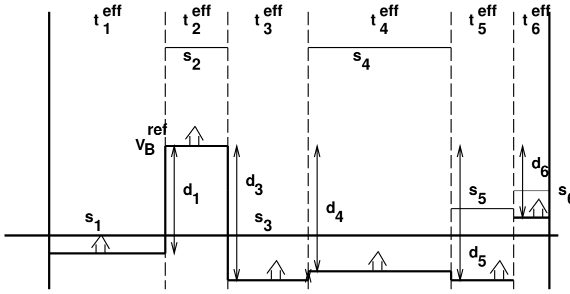

Figure 2: An average cycle for an nFET which when repeated over and over models the behavior of the body over a long period of time.

It is important to note that both the displacements d_i and the relaxation times τ_i are body-bias dependent; that is, both d_i and τ_i are functions of V_B^{ref} so that Equation 3 must be solved self-consistently. The body-voltage dependencies of d_i and τ_i are modelled as simple polynomial curve fits to circuit simulation results, since the relationships are too complex to motivate physically-based formulae. (We actually fit to the logarithm of τ_i, since τ_i varies over several orders of magnitude.) We find that both the τ_i and d_i are independent of device width, W. d_i is independent of W because the dominant components of capacitance scale proportionately with W. Moreover, τ_i is independent of W because both the body currents and body capacitance scale proportionately with W.

We let V_j^{zero} denote the steady-state reference voltage in state j, $V_j^{zero} = s_j - d_j$. Also, above (below) a certain value of V_B^{ref} for the nFET (pFET), one or both of the source-body or drain-body junctions become strong forward biased (which we consider to be at biases greater than 0.6 V). We refer to the reference voltage at which this occurs as $V_j^{forward}$ for state j.

We note that, at a supply voltage of 2.5V in our example technology, $V_6^{forward} = V_6^{zero}$ because of the dominating effect of the on-state impact ionization current at this supply voltage. This current is so large that a strongly forward-biased junction is required to balance it in steady-state. This means that whenever the device spends any time in state 6 at this supply, the steady-state reference body voltage is immediately (within a microsecond) pinned at $V_6^{forward} = V_6^{zero}$.

The model of Figure 1 and Equation 3 provides for both initial-condition and steady-state body-voltage analysis. We consider four types of estimation. As is traditionally done in static analysis, each has associated with it minimum and maximum possible values that bound all of the remaining unknowns, the body voltage *uncertainty*.

Full-uncertainty body-voltage estimation. This applies when there is no knowledge of the switching activity of the circuit and one must be assured that the uncertainty covers all possible stimulus and history. One considers a given state j to be accessible if $t_j^{eff} > 0$ for that state. The dynamic state 6 is considered accessible if more than one of the states 1, 2, and 5 are accessible, since switching events between these states almost always involves transiently passing through state 6. Let $\mathcal{A}$ denote the set of all accessible states, and let $\mathcal{A}_{static}$ denote the set of all accessible static states. In the full-uncertainty case, one assumes that the FET can spend an indeterminant amount of time in any accessible state. In this case, the maximum (minimum) body voltage is the maximum (minimum) value of V_j^{zero} across all accessible states. For the nFET and pFET, the minimum and maximum body voltages are then given by $(V_B^{ref})_{min} = \min_{j\in\mathcal{A}} V_j^{zero}$ and $(V_B^{ref})_{max} = \max_{j\in\mathcal{A}} V_j^{zero}$, respectively.

Initial-condition body-voltage estimation. This applies for times in an initial period of switching activity after a long period of quiescence. In this case, one assumes that the FET has reached a dc steady state in any accessible *static* state (i. e., states 1 through 5). For the nFET and pFET, the minimum and maximum body voltages are then given by $(V_B^{ref})_{min} = \min_{j\in\mathcal{A}_{static}} V_j^{zero}$ and $(V_B^{ref})_{max} = \max_{j\in\mathcal{A}_{static}} V_j^{zero}$, respectively. We do not consider state 6 here because it can only be reached as part of a switching event and does not contribute to the body voltage "near" dc quiescence. The uncertainty comes about because we have assumed that we do not know the specific quiescent state of the circuit.

Accessibility steady-state body-voltage estimation. This applies to the case that the circuit is under unknown but steady switching activity. In this case, we take advantage of the fact that for the nFET (pFET), V_B^{ref} can not be greater (smaller) than the largest (smallest) value of $V_j^{forward}$ in any accessible state j; otherwise, the body would rapidly discharge. This, of course, assumes that all accessible states are visited with reasonable frequency. Furthermore, for the nFET (pFET), the smallest (largest) V_B^{ref} can be is the smallest (largest) value of V_j^{zero} in any accessible state j. Therefore, in this analysis, if we know the FET is under reasonably steady switching activity in which all accessible states are visited, the minimum and maximum body voltages for the nFET are given by $(V_B^{ref})_{min} = \min_{j\in\mathcal{A}} V_j^{zero}$ and $(V_B^{ref})_{max} = \min_{j\in\mathcal{A}} V_j^{forward}$, respectively. For the pFET, the minimum and maximum body voltage are given by $(V_B^{ref})_{min} = \max_{j\in\mathcal{A}} V_j^{forward}$ and $(V_B^{ref})_{max} = \max_{j\in\mathcal{A}} V_j^{zero}$, respectively. The uncertainty of accessibility estimation can be reduced if one is further willing to restrict the allowable waveforms to those meeting known timing requirements and known signal probabilities.

Detailed steady-state body-voltage estimation. This applies to the case in which the circuit is under switching activity that can be quantified logically with known signal probabilities and temporally with known arrival times. We tighten up the steady-state body-voltage uncertainty provided by accessibility analysis by determining the maximum and minimum possible V_B^{ref} values from Equation 3 with consideration of *all* of the t_i^{eff}. To maximize V_B^{ref}, one must maximize the time in those states with higher V_j^{zero}; similarly, to minimize V_B^{ref}, one must maximize the time in those states with lower V_j^{zero}. To formalize this, we define the rank of the state i as an integer r_i indicating the priority of states to maximize the body voltage. We can also define a complementary rank $\overline{r}_i$ for minimizing V_B^{ref}; these priorities are simply the reverse of the maximum case. One's ability to favor the t_i^{eff} of given states in detailed body-voltage estimation is limited by additional constraints derived from static timing analysis and stochastic techniques, as described later in this section.

3.2 Determining the accessible states and allowable values of t_i^{eff}

To determine the accessible states $\mathcal{A}$ for a given FET as well as to determine allowable values of t_i^{eff} for detailed steady-state analysis, we need information about the circuit environment of each transistor, both logical and temporal.

We characterize the logical environment of each FET by a set of signal probabilities which determine the possible states of the source, gate, and drain of the transistor at the end of a cycle. For the nFET, we define the probabilities (or conditional probabilities) $P(G)$, $P(D|\overline{G})$, $P(\overline{D}|\overline{G})$, $P(S|\overline{G})$, $P(\overline{S}|\overline{G})$, $P(S|G) = P(D|G)$, and $P(\overline{S}|G) = P(\overline{D}|G)$. $P(S|\overline{G})$, for example, is the probability that at the end of a cycle the source is driven high given that the gate is low. There are analogous probabilities for the pFET with $\overline{G}$ taking the place of G. Accessibility of a state can be immediately determined from these probabilities. For example, nFET state 1 is accessible if $(P(G) > 0) \bigwedge (P(S|G) < 1)$.

To calculate the t_i^{eff} necessary for detailed steady-state analysis, we need to use these FET signal probabilities to calculate the transition probabilities, $P_{i \to j}$, the probability that a given FET in a given cycle is transitioning from state i to state j. To find these transition probabilities, we begin by noting that the cycle-to-cycle transitions through the state diagram in Figure 1 represents a Markov process with six-by-six transition matrix $\mathbf{A}$. Assigning different transition matrices to the minimum and maximum cases yields the difference equations $(P_i^{max})_{k+1} = \mathbf{A}_{max}(P_i^{max})_k$ and $(P_i^{min})_{k+1} = \mathbf{A}_{min}(P_i^{min})_k$, where the matrix $\mathbf{A}_{max/min}$ has each column given by

$$(p_1^{max/min} p_2^{max/min} p_3^{max/min} p_4^{max/min} p_{5a}^{max/min} p_{5b}^{max/min})^T$$

$(P_i)_k$ is the probability of being in state i at the end of cycle k. p_i is the probability of making a transition to state i and follow directly from the source, gate, and drain signal probabilities. For example, for the nFET, $p_3^{max} = (1 - P(G))P(\overline{S}|\overline{G})P(\overline{D}|\overline{G})$ while $p_3^{min} = (1 - P(G))(1 - P(S|\overline{G}))(1 - P(D|\overline{G}))$. The maximum (minimum) case assumes that the floating node condition on the source or drain takes a high (low) voltage value. Diagonalizing A (trivially) and finding the eigenvector associated with eigenvalue 1 (normalized so that the sum of the elements of the vector is 1) gives the steady-state values of the P_i. From these probabilities, one can calculate a set of thirty-six transition probabilities for both the minimum or maximum cases: $P_{i \to j}^{max/min} = P_i^{max/min} p_j^{max/min}$.

Calculating the t_i^{eff} for detailed steady-state analysis involves determining not only the probability of making a transition in a given cycle but the fraction of the cycle time $(t_i^{j \to k})$ that can be spent in each state i as part of a given transition $j \to k$. In particular, we seek the values of $t_i^{j \to k}$ to maximize and minimize the body voltage among the set of possible waveforms. To do this, we require temporal information, in particular early and late arrival times (rising and falling) for the source, gate, and drain of the FET under consideration (the target FET). We denote these arrival times for the early case as:

- S_{rise}^{early}, D_{rise}^{early}, G_{fall}^{early}. Earliest times the source, drain, gate of the FET can be driven high.
- S_{fall}^{early}, D_{fall}^{early}, G_{rise}^{early}. Earliest times the source, drain, gate of the FET can be driven low.

There are comparable arrival times associated with the late state: S_{rise}^{late}, S_{fall}^{late}, D_{rise}^{late}, D_{fall}^{late}, G_{fall}^{late}, and G_{rise}^{late}. For the source and drain arrival time, we are assuming that the target FET is off. The details of how these are obtained in the context of static timing analysis is described in Section 4. Each transition has associated with it a set of arrival times necessary to make that transition, a *transition set*, denoted as $\mathcal{T}_{i \to j}$. For example, for the $1 \to 2$ transition for the nFET, the associated arrival time set is $\mathcal{T}_{1 \to 2} = \{S_{rise}, D_{rise}\}$. For $1 \to 4$ for the nFET, the associated arrival time set is $\mathcal{T}_{1 \to 4} = \{G_{fall}, S_{rise}, D_{rise}\}$. We can define max and min operators which act on the transition sets. $\max(\mathcal{T}_{i \to j})$ returns the largest of the early arrival times in the transition set, while $\min(\mathcal{T}_{i \to j})$ returns the smallest of the late arrival times in the transition set.

To indicate the states of Figure 1 involved in a cycle and to handle the possibility of hazards, we can denote the waveform in a cycle (in this case involving a transition from i to j) using the *transition notation* $i \overset{max}{\to} k \overset{min}{\to} j$. In this cycle, a hazard to state k occurs as part of the transition. The transition notation must involve only static states and indicates the amount of time spent in each of these static states as part of the transition. Specifically for this example, $t_i^{i \to j} = \max(\mathcal{T}_{i \to k})$, $t_k^{i \to j} = \min(\mathcal{T}_{k \to j}) - \max(\mathcal{T}_{i \to k})$, and $t_j^{i \to j} = t_{cycle} - \min(\mathcal{T}_{k \to j})$. Hazards are introduced when they act to increase (in the case that we are seeking the maximum body voltage) or decrease (in the case that we are seeking the minimum body voltage) the steady-state body voltage that would result from the particular waveform being repeated indefinitely. Specifically, a state k can be inserted between states i and j according to one of the following cases.

Case I. If $(r_k > r_i) \bigwedge (r_k > r_j) \bigwedge (\max(\mathcal{T}_{i \to k}) < \min(\mathcal{T}_{k \to j}))$, the state k can be inserted between i and j as a hazard to increase the steady-state body voltage. The cycle after this insertion is $i \overset{max}{\to} k \overset{min}{\to} j$. In this case, increasing the amount of time in state k at the expense of states i and j increases the body voltage. If $(\overline{r}_k > \overline{r}_i) \bigwedge (\overline{r}_k > \overline{r}_j) \bigwedge (\max(\mathcal{T}_{i \to k}) < \min(\mathcal{T}_{k \to j}))$, the state k can be inserted between i and j as a hazard to decrease the body voltage. The cycle after this insertion is the same as in the maximum case. However, in this case, increasing the amount of time in state k at the expense of states i and j decreases the body voltage.

Case II. If $(r_k > r_j) \bigwedge (r_k < r_i) \bigwedge (\min(\mathcal{T}_{i \to k}) \geq \min(\mathcal{T}_{i \to j})) \bigwedge (\min(\mathcal{T}_{k \to j}) > \min(\mathcal{T}_{i \to k}))$, the state k can be inserted between i and j as a hazard to increase the body voltage. In this case, the initial cycle is $i \overset{min}{\to} j$. After insertion, it is $i \overset{min}{\to} k \overset{min}{\to} j$. State k is inserted only if adding it does not decrease the time in state i. If $(\overline{r}_k > \overline{r}_j) \bigwedge (\overline{r}_k < \overline{r}_i) \bigwedge (\min(\mathcal{T}_{i \to k}) \geq \min(\mathcal{T}_{i \to j})) \bigwedge (\min(\mathcal{T}_{k \to j}) > \min(\mathcal{T}_{i \to k}))$, the state k can be inserted between i and j as a hazard to decrease the body voltage. The cycle before and after insertion is the same as in the maximum case.

Case III. If $(r_k > r_i) \bigwedge (r_k < r_j) \bigwedge (\max(\mathcal{T}_{k \to j}) \leq \max(\mathcal{T}_{i \to j})) \bigwedge (\max(\mathcal{T}_{k \to j}) > max(\mathcal{T}_{i \to k}))$, state k can be inserted between i and j as a hazard to increase the body voltage. Initially the cycle is $i \overset{max}{\to} j$. After insertion, it is $i \overset{max}{\to} k \overset{max}{\to} j$. State k is inserted only if adding it does not decrease the time in state j. If $(\overline{r}_k > \overline{r}_i) \bigwedge (\overline{r}_k < \overline{r}_j) \bigwedge (\max(\mathcal{T}_{k \to j}) \leq \max(\mathcal{T}_{i \to j})) \bigwedge (\max(\mathcal{T}_{k \to j}) > max(\mathcal{T}_{i \to k}))$, state k can be inserted between i and j as a hazard to decrease the body voltage. The cycle before and after insertion is the same as in the maximum case.

These preliminaries lead to a straightforward algorithm for determining the $t_k^{i \to j}$ to maximize or minimize the body voltage for a given transition. For the maximum case (the minimum case is the same except the complementary ranks $\overline{r}_i$ are used):

1. If $r_j > r_k$, then the starting cycle is $j \overset{min}{\to} k$ else the starting cycle is $j \overset{max}{\to} k$.
2. Find the accessible state k' with the largest rank (different from j and k and not previously inserted or attempted) that can be inserted between states j and k, If no such state exists, then exit with the current cycle. However, if such a state exists then the new cycle is either $j \overset{max}{\to} k' \overset{min}{\to} k$, $j \overset{max}{\to} k' \overset{max}{\to} k$, or $j \overset{min}{\to} k' \overset{min}{\to} k$, depending on which case led to the insertion.
3. Repeat step 2 for each transition in the current average cycle. Repeat this until no further refinement is possible.

For the purposes of detailed steady-state body-voltage estimation, we assume that if state 6 is accessible, exactly one switching event through 6 occurs per cycle and assign a small switching time to each $t_6^{i \rightarrow j}$. We find that, in practice, the detailed results are not very sensitive to the exact value of $t_6^{i \rightarrow j}$, just that there is some nonzero time in state 6.

From the $t_i^{j \rightarrow k}$ determined above, we can calculate an effective amount of time (t_i^{eff}) on the average per cycle that the FET is in the state i:

$$(t_i^{eff})^{max/min} = \sum_{j,k} P_{j \rightarrow k}^{max/min} (t_i^{j \rightarrow k})^{max/min}$$

Obviously, there are two sets of t_i^{eff} values, one to maximize and one to minimize the body voltage. These determine the uncertainty of the detailed steady-state body voltage estimate.

4 Static timing analysis

We have incorporated this body voltage characterization into a prototype static transistor-level timing analysis engine, SOISTA [for SOI Static Timing Analyzer]. The design is partitioned into channel-connected components (CCCs) for analysis, as is traditionally done in static transistor-level tools [7]. SOISTA utilizes a breadth-first search (BFS) of the resulting timing graph and propagates signal probabilities using assumptions of spatial and temporal independence, borrowing from similar techniques in static power analysis [12]. Signal probabilities can be easily propagated from CCC inputs to outputs using basic probability theory [13] or BDD analysis [12, 14]. Uncertainty is built into the timing analysis to account for variations in the effective gate input capacitance depending on the switched state of the gate (*loading uncertainty*).

Once the signal probabilities and arrival times are known at the inputs of a CCC, these probabilities are translated into the FET signal probabilities and arrival time values for detailed body-voltage estimation. We first consider the calculation of the signal probabilities. If we let i and j denote two channel nodes of the CCC, then similar to [15], we can define the kth *path* $P_{i,j}^k$ as one connection of FETs between i and j. We can also define a *path function* $f_{P_{i,j}^k}$ as a Boolean function indicating whether the kth path is conducting. Let n_i denote a controlling nFET gate input function in the path, and let p_i denote a controlling pFET gate input function in the path. Then, the path function is given by $f_{P_{i,j}^k} = \bigwedge_{n_i \in P_{i,j}^k} n_i \wedge \bigwedge_{p_i \in P_{i,j}^k} \overline{p_i}$. If there are N paths between i and j, then the total path function $f_{P_{i,j}}$ is given by $f_{P_{i,j}} = \bigvee_{\forall P_{i,j}^k} f_{P_{i,j}^k}$. The path probability $P(P_{i,j})$, the probability that at the end of the cycle, the path from i to j is conducting, follows from elementary probability theory or BDD analysis [12]. The source and drain conditional probabilities required for the detailed body voltage estimation are given by specific path probabilities. For example, $P(D|\overline{G})$ is the path probability between the drain node and V_{DD} with the gate of the target transistor low.

We next consider calculating the FET arrival times which determine the temporal circuit environment of each FET. G_{fall}^{early}, G_{rise}^{early}, G_{fall}^{late}, G_{fall}^{early} are determined directly from the CCC arrival times. To determine S_{rise}^{early}, D_{rise}^{early}, D_{rise}^{late}, S_{rise}^{late}, we trace all paths from the channel node (node i) to V_{DD} (node 1) with the target transistor off.

$$\forall P_{i,1} : S_{rise}^{early} = min\left(\forall n_i, p_i \in P_{i,1} : (G_{rise}^{early})_{n_i}, (G_{fall}^{early})_{p_i}\right)$$

$$\forall P_{i,1} : S_{rise}^{late} = max\left(\forall n_i, p_i \in P_{i,1} : (G_{rise}^{late})_{n_i}, (G_{fall}^{late})_{p_i}\right)$$

with identical expressions for D_{rise}^{early} and D_{rise}^{late}. These relations determine the earliest or latest time a conducting path from node i to V_{DD} can be established if at the beginning of the cycle no such path exists. Similarly, to determine S_{fall}^{early}, D_{fall}^{early}, D_{fall}^{late}, S_{fall}^{late}, we trace all paths from the channel node (node i) to ground (node 0) with the target transistor off. In cases in which there are no paths, we set early arrival times to t_{cycle} and late arrival times to 0.

5 Results and discussion

We present static timing results from SOISTA for three examples (of increasing complexity) and compare these with the results of circuit simulations in which vectors are chosen both to correctly sensitize the delay path in question and to match the assumed signal probabilities. At the 2.5-V supply, the accessibility results exactly match the detailed steady-state results because of the 6-state pinning; therefore, separate accessibility results are not presented for the larger supply.

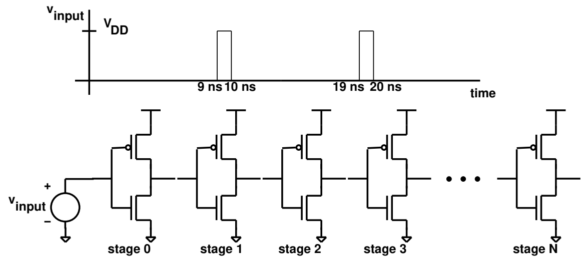

Figure 3: Chain of identical inverters simulated with the waveform shown in the inset.

5.1 Inverter chain

The first is a chain of identical inverters as shown in Figure 3 stimulated with the periodic waveform shown in the inset. The input waveform repeats every 10 nsec and is equivalent to a signal probability of 0.1 on the input of even-stage inverters and 0.9 on the input of odd-stage inverters. Before $t = 0$, even (odd) stages have a zero (one) on their input. We consider results at two supplies, 2.5 V in Figure 4 and 1.0 V in Figure 5. In Figure 4(a), we present the body voltages for the FETs as determined by circuit simulation for both even (in solid lines) and odd (in dashed lines) inverter stages. We notice that initially the even-stage FETs have higher body voltages than the odd-stage FETs. This is because the even-stage FETs have their gates held low before $t = 0$ with the pFET (nFET) in state 2 (5), while the odd-stage FETs have their gates held high before $t = 0$ with the pFET (nFET) in state 5 (1). $r_5 > r_1$ for the nFET and $r_2 > r_5$ for the pFET. As shown in the stage delay results in Figure 4(b) (even stage delay in solid, odd-stage delay in dashed), this gives the even stages initially a longer rise time but smaller fall time than the odd stages. Initially, then the input pulses are stretched [16] as they move down the inverter chain. As switching begins, state 6 becomes accessible and the body voltages become pinned in about a microsecond (the time scale of τ_6) to s_6. We also note that, in this case, the steady-state nFET (pFET) body voltage is slightly less (more) than the initial-condition minimum (maximum) value. 6-state pinning means that there is no difference between the steady-state body voltages of the FETs in even and odd stages. In steady-state, then, the rise and fall delays become the same in the even and odd stages and there is no pulse stretching.

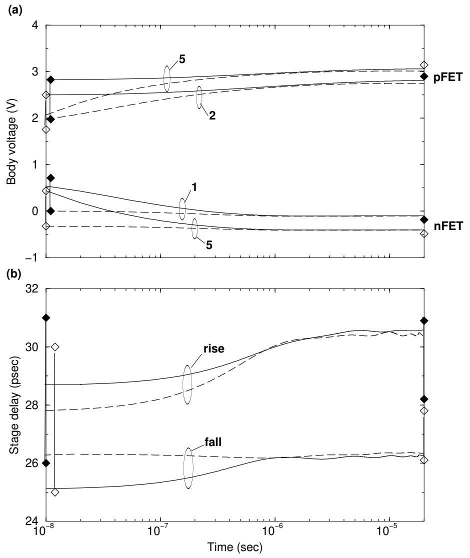

Figure 4: Inverter chain results at 2.5-V supply. (a) Body voltages from circuit simulation for even (solid lines) and odd (dashed lines) inverter stages. (b) Inverter delay.

We now consider how these results compare with SOISTA. Early and late arrival times at the input of the chain, both rise and fall, are set to 100 psec. The rise and fall times at the input of the chain are also set to 100 psec. The diamonds on the right vertical axes in Figures 4(a) and 5(a) correspond to the steady-state body-voltages estimated by SOISTA for an input signal probability of 0.1, propagated as 0.9 to the inputs of the odd stages. State 1 and state 2 for the pFET and nFET, respectively, are shown as solid diamonds. State 5 for the pFET and nFET are shown as hollow diamonds. The minimum and maximum values of the steady-state body voltage for these cases are indistinguishably close because there is no path delay variation to produce any significant differences between the early and late arrival times. At 2.5 V supply, 6-state pinning during steady-state causes the detailed body voltages to be the same for even and odd stages, while at the 1.0-V supply, the absence of 6-state pinning causes disparate steady-state voltages between even and odd stages. The diamonds slightly to the left of the right vertical axis in Figure 5(a) are the minimum and maximum body voltages determined by SOISTA from accessibility analysis. These numbers bound the full steady-state body-voltage variation of both even and odd stages. On the left vertical axis, we show the minimum and maximum initial-condition body voltage values estimated by SOISTA. These bound almost precisely the initial condition body voltages observed in the dynamic simulation, since in this case, the dynamic simulation covers all the accessible state states. In Figures 4(b), 5(b), the SOISTA steady-state delays bound those determined by dynamic simulation. All of the uncertainty in this case is associated with the loading uncertainty, since the body voltage is nearly precisely predicted by SOISTA. The delays determined by SOISTA with accessibility analysis are also noted in Figure 5(b). The initial-condition stage delays also bound the actual initial-condition stage delays of the dynamic simulation. In this case, the uncertainty comes from both the loading uncertainty and the body-voltage uncertainty.

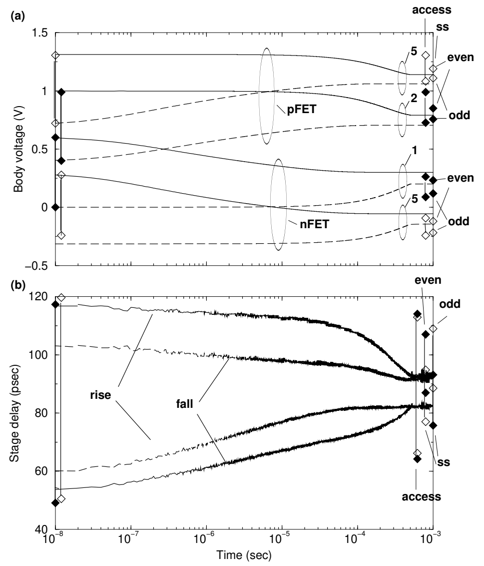

Figure 5: Inverter chain results at 1.0-V supply. (a) Body voltages from circuit simulation for even (solid lines) and odd (dashed lines) inverter stages. (b) Inverter delay.

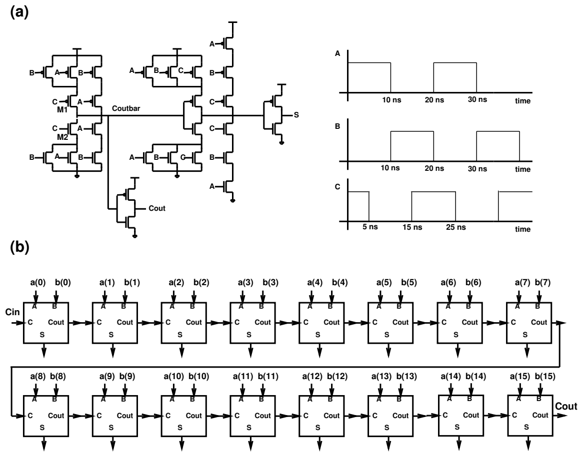

Figure 6: 16-bit ripple-carry adder circuit: (a) the associated full-adder circuit and (b) the connection of the full-adder cells. The inset of (a) gives the waveform applied for dynamic simulation.

5.2 Ripple-carry adder

The next example we consider is a static 16-bit ripple carry adder shown in Figure 6(b). Figure 6(a) shows the component full-adder circuit. In the circuit simulation, we use the input waveforms shown in the inset of Figure 6(a), which sensitizes the critical path of this circuit, the carry chain. The "A" waveform is applied to each A input and the "B" waveform is applied to each B input. The "C" waveform is applied to the Cin input of the ripple-carry (see Figure 6(b)). These waveforms correspond to signal probabilities of 0.5 on the A and B inputs of each full-adder cell and 0.5 on the C input of each full-adder cell. For these input signal probabilities, the signal probability of $Cout$ is 0.5, so that each cell sees identical switching activity. Before $t = 0$, A and C are high and B is low for each cell. Figure 7 shows the results for a supply voltage of 2.5 V.

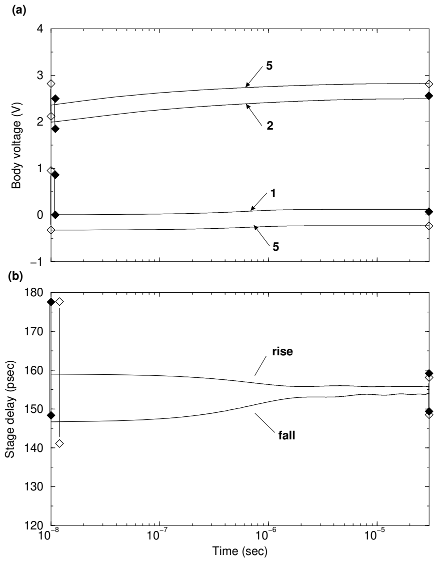

Figure 7: Carry chain results at 2.5-V supply. (a) Body voltages for $M1$ and $M2$. (b) Full-adder cell delay.

In Figure 7(a), we compare the body voltages of transistors $M1$ and $M2$ of Figure 6(a) with the SOISTA initial condition and detailed steady-state results. (The detailed steady-state results match the accessibility steady-state results because of the 6-state pinning.) The $M1$ curve labelled 5 (2) and $M2$ curve labelled 1 (5) correspond to the case in which C is high (low) for a given cell. The steady-state values match almost exactly the values determined from circuit simulation. They have negligibly small uncertainty because the difference between the early and late arrival times is a small fraction of t_{cycle}. The initial-condition body-voltage values bound the circuit simulation results. The simulation results match exactly the lower bound for transistor M2 because the simulation begins with M2 in state 1, which determines the minimum possible initial-condition value. M1, by contrast, begins in state 5 which is neither the minimum (state 3) nor maximum (state 4) accessible state ($\mathcal{A}_{static} = \{1, 3, 5, 4\}$). Therefore, the M1 initial condition values from simulation lie within the SOISTA-determined ranges. Figure 7(b) shows the complete stage delay of the full adder cell from C to $Cout$ for both rising and falling $Cout$. The steady-state and initial-condition delays from SOISTA bound the simulation values. The uncertainty of the steady-state values derives entirely from the loading uncertainty.

5.3 4-2 compressor

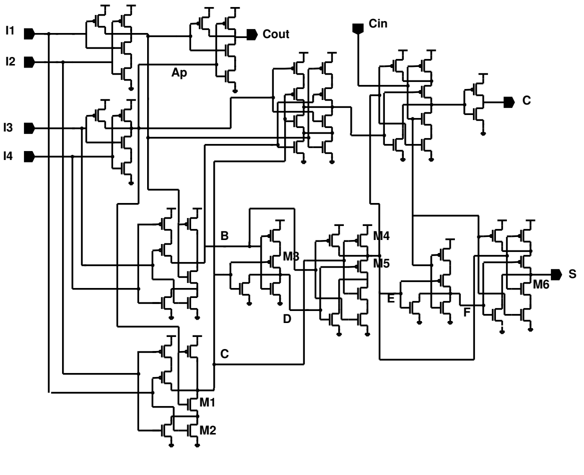

Figure 8: 4-2 compressor circuit

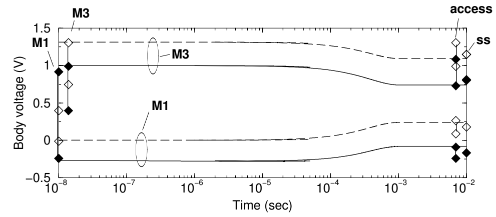

Figure 9: Body voltages for $M1$ and $M3$ of 4-2 compressor circuit at 1.0-V supply.

The last, and most complex, example presented here to compare the SOISTA and circuit simulation results is a 4-2 compressor circuit from a tree multiplier design [17] (see Figure 8). We specifically consider the long delay path, I4-Ap-C-D-E-F-S, and the short delay path, I2-C-E-S. In Figure 9, we present body-voltage results for two FETs ($M1$ and $M3$) along the long path at the 1.0-V supply. The dashed (solid) curves for $M3$ correspond to the case in which the gate is high (low) and the FETs are in state 5 (2). The dashed (solid) curves for $M1$ correspond to the case in which the gate is high(low) and the FET is in state 1 (5). The diamonds on the left vertical axis give the SOISTA-determined initial condition body voltages for these same conditions. We note that at the dc state established in the circuit simulation before t = 0, I1 = I3 = 0, I2 = I4 = Cin = 1.0 V. At these values, we find C = 0, B = 0. Therefore, M3 is in state 4 and M1 is in state 1. For the static accessible sets of M1 and M3 ($\mathcal{A}_{static} = \{5, 1, 3, 4\}$ for M3 and $\mathcal{A}_{static} = \{1, 2, 4, 5\}$ for M1), these represent the states of highest and lowest reference body voltage, respectively. Therefore, these curves match the maximum (for M3) and minimum (for M1) body voltage values calculated by SOISTA. On the right vertical axis, we show the steady-state detailed body voltage associated with the longest path sensitization. As expected for the late-mode case, these are slightly less than the simulation values for the nFET and slightly greater than the simulation values for the pFET. We also show the body-voltage estimates from accessibility analysis, which quite expectedly bound the detailed results. In Table 1, we compare the initial-condition delays determined by circuit simulation with the SOISTA-determined initial-condition delays. Table 2 does a similar comparison between the steady-state delays

	SOISTA initial				SPICE initial			
	Rise		Fall		short-path		long-path	
	max	min	max	min	rise	fall	rise	fall
I2	100	100	100	100	100	100	100	100
I4	100	100	100	100	100	100	100	100
Ap	285	229	398	284			235	315
C	645	318	576	320	326	379	476	432
D	878	450	946	501			723	553
E	1341	531	1200	537	629	762	785	943
F	1602	661	1366	618			1112	936
S	1842	681	1905	662	1064	837	1104	1174

Table 1: SOISTA-determined initial-condition delays versus circuit simultaion delays.

	SOISTA detailed				SPICE steady-state			
	Rise		Fall		short path		long path	
	max	min	max	min	rise	fall	rise	fall
I2	100	100	100	100	100	100	100	100
I4	100	100	100	100	100	100	100	100
Ap	264	264	310	310			250	302
C	520	363	444	375	377	388	511	424
D	699	575	640	463			666	616
E	950	725	874	703	743	723	904	819
F	1054	853	1125	871			1000	1076
S	1255	953	1154	960	989	975	1211	1098

Table 2: SOISTA-determined detailed steady-state delays versus circuit simulation delays.

determined by circuit simulation (after more than 50,000 cycles of simulation) and the SOISTA-determined detailed steady-state delays. In all cases, the SOISTA-determined delays bound the SPICE delays. One should also notice the considerable reduction in uncertainty between the initial-condition and detailed steady-state delays, as the component of this uncertainty due to body voltage variation is noticeably reduced. (The remaining uncertainty is due primarily to delay-path variation and loading uncertainty.)

6 Conclusions and future work

In this paper, we have presented a circuit-focussed model of the floating-body potential of PD-SOI FETs. This model allows one to determine the body voltage and its associated uncertainty, depending on knowledge of the switching activity of the FETs in question. Four types of estimation are possible depending on switching assumptions and the amount of information known about the logical and temporal environment of the circuit under analysis. We have incorporated this model into a prototype transistor-level static timing analysis engine to demonstrate the impact reduced body-voltage uncertainty can have on performance evaluation. We find that the body-voltage uncertainty can be significantly reduced with fairly conservative assumptions about switching behavior.

Future work will include incorporating these body voltage estimates into transistor-level static noise analysis. In addition, we intend to consider design techniques whereby a normally inactive block could be periodically stimulated to keep it "primed" so that when it is eventually exercised, it has more tightly predictable body voltage variation. This is similar to some of the circuit techniques which attempt to force discharge of the body during "non-critical" periods of circuit operation (e.g. precharge in dynamic logic) to reduce parasitic bipolar leakage. In many ways, this could also be viewed as analogous to DRAM refresh. More work will be required to determine the necessary frequency and nature of this pattern.

The work was supported by the National Science Foundation under grant CCR-97-34216 and by a gift from the IBM Corporation under the University Partnership Program. We gratefully acknowledge C. T. Chuang, R. Puri, G. Sai-Halasz, and M. R. Rosenfield of IBM Yorktown for encouragement, helpful discussions, and preprints of their work.

References

[1] C. T. Chuang, P.-F. Lu, and C. J. Anderson. SOI for digital CMOS VLSI: Design considerations and advances. *Proceedings of the IEEE*, 86:689 – 720, 1998.

[2] C. T. Chuang and R. Puri. SOI digital CMOS VLSI – a design perspective. In 36^{th} *ACM/IEEE Design Automation Conference*, pages 709 – 714, 1999.

[3] J. Gautier and J. Y.-C. Sun. On the transient operation of partially depleted SOI NMOSFET's. *IEEE Electron Device Letters*, 16:497 – 499, 1995.

[4] L. T. Su, J. B. Jacobs, J. Chung, and D. A. Antoniadis. Deep-submicrometer channel design in silicon-on-insulator (SOI) MOSFETs. *IEEE Electron Device Letters*, 15(5):183 – 185, 1994.

[5] R. Puri and C. T. Chuang. Hysteresis effect in pass-transistor-based partially-depleted SOI CMOS circuits. In *Proceedings of the International SOI Conference*, 1998.

[6] M. M. Pelella, C. T. Chuang, J. G. Fossum, C. Tretz, B. W. Curran, and M. G. Rosenfield. Hysteresis in floating-body PD/SOI circuits. In *Proc. Tech. Papers, Int. Symp. on VLSI Technology, Systems, and Applications, Taipei, Taiwan*, 1999.

[7] N. P. Jouppi. Timing analysis and performance improvement of MOS VLSI designs. *IEEE Trans. CAD*, 6:650 – 665, 1987.

[8] K. L. Shepard, V. Narayanan, and R. Rose. Harmony: Static noise analysis for deep-submicron digital integrated circuits. *IEEE Trans. CAD*, pages 1132–1150, August 1999.

[9] BSIM3SOI Manual. Technical report, University of California, Berkeley, 1998. Version 1.3.

[10] G. G. Shahidi et al. SOI for 1-volt CMOS technology and applictaion to a 512kb SRAM with 3.5 ns access time. In *Proceedings of the IEDM*, pages 813 – 816, 1993.

[11] S. A. Parke, J. E. Moon, H. C. Wann, P. K. Ko, and C. Hu. Design for suppression of gate-induced drain leakage in LDD MOSFETs using a quasi-two-dimensional analytical model. *IEEE Transactions on Electron Devices*, 39(7):1697 – 1703, 1992.

[12] Farid N. Najm. A survey of power estimation techniques in VLSI circuits. *IEEE Transations on VLSI Systems*, 2:446 – 455, 1994.

[13] Athanasios Papoulis. *Probability, random variables, and stochastic processes*. McGraw-Hill, New York, 1991.

[14] Randal E. Bryant. Graph-Based Algorithms for Boolean Function Manipulation. *IEEE Trans. CAD*, 35:677–691, 1986.

[15] A. Kuehlmann, A. Srinivasan, and D. P. Lapotin. Verity – a formal verification program for custom CMOS circuits. *IBM Journal of Research and Development*, 39(1/2):149 – 165, 1995.

[16] A. Wei, D. A. Antoniadis, and L. A. Bair. Minimizing floating-body-induced threshold voltage variation in partially depleted SOI CMOS. *IEEE Electron Device Letters*, 17:391 – 394, 1996.

[17] G. Goto, T. Sato, M. Nakajima, and T. Sukemura. A 54-by-54-b regularly structured tree multiplier. *IEEE Journal of Solid-State Circuits*, 27:1229, 1992.