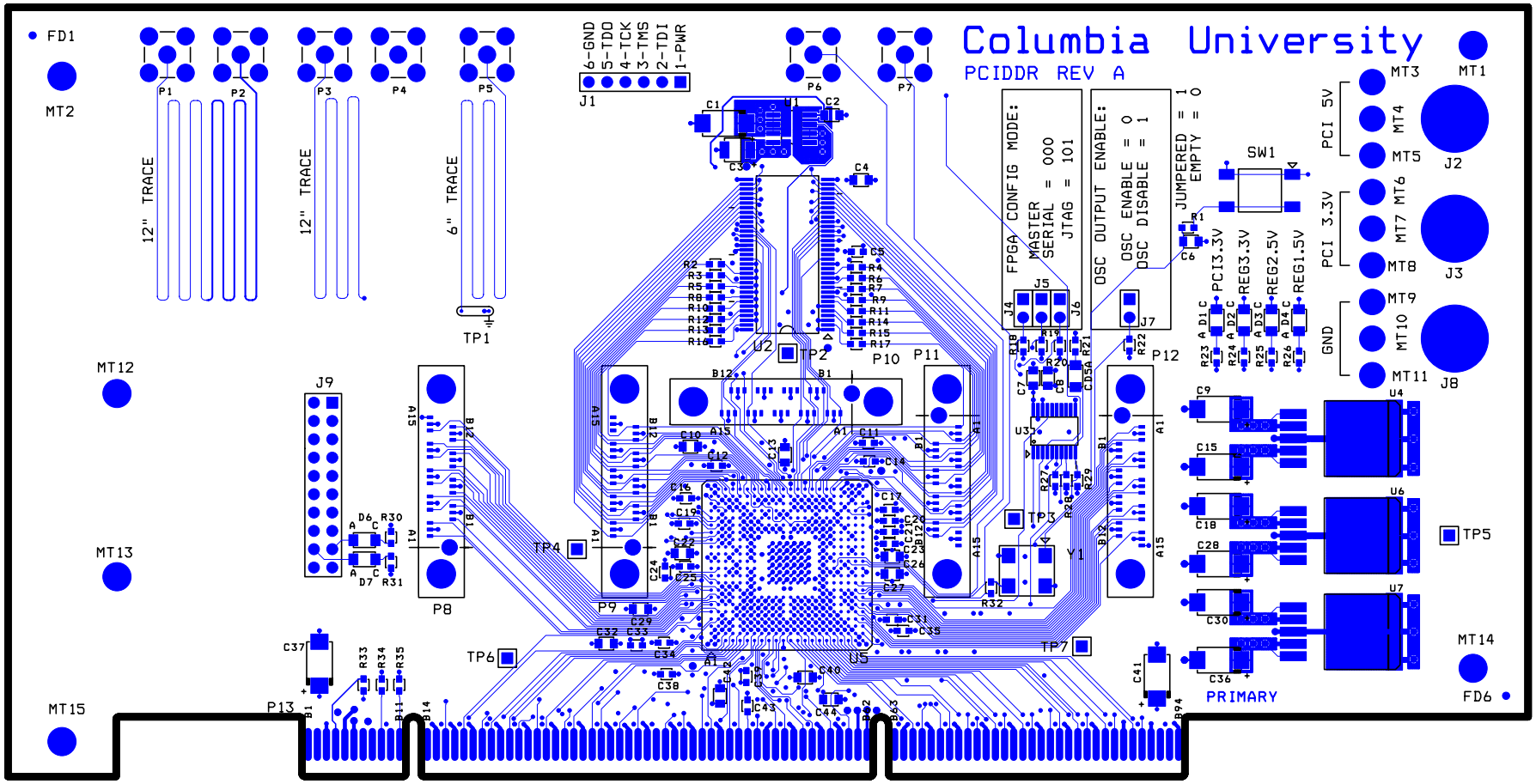
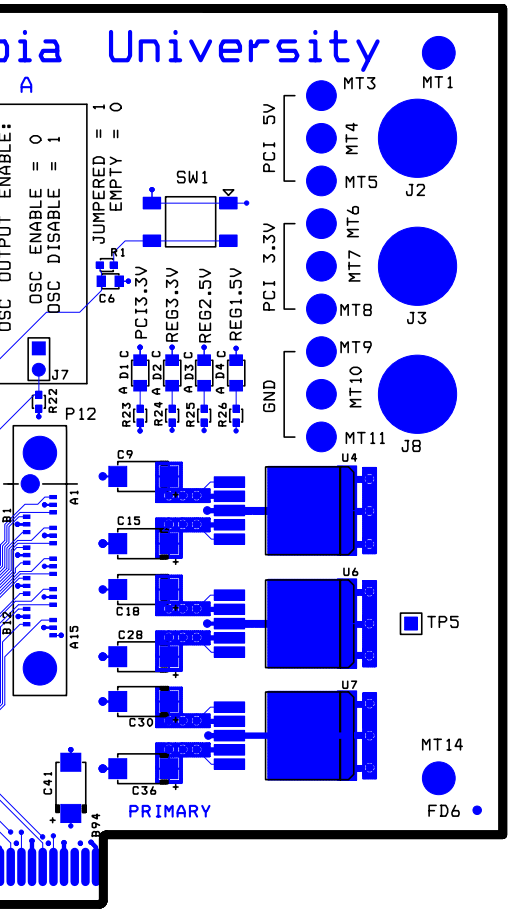

Columbia University
PCIDDR REV A
FD1
MT2
MT12
MT13
MT15
MT1
MT3
MT4
MT5
MT6
MT7
MT8
MT9
MT10
MT11
MT14
FD6
12" TRACE
12" TRACE
6" TRACE
TP1
TP2
TP3
TP4
TP5
TP6
TP7
J1
6-GND
5-TDO
4-TCK
3-TMS
2-TDI
1-PWR
J2
J3
J8
PCI 5V
PCI 3.3V
GND
SW1
FPGA CONFIG MODE:
MASTER = 000
SERIAL = 101
JTAG
OSC OUTPUT ENABLE:
OSC ENABLE = 0
OSC DISABLE = 1
JUMPERED = 1
EMPTY = 0
PC13.3V
REG3.3V
REG2.5V
REG1.5V
PRIMARY
J9
P8
P9
P10
P11
P12
P13
U1
U2
U3
U4
U5
U6
U7
Y1


bia University
A
OSC OUTPUT ENABLE:
OSC ENABLE = 0
OSC DISABLE = 1
JUMPERED = 1
EMPTY = 0
SW1
R1
C6
J7
R22
P12
PCI3.3V
REG3.3V
REG2.5V
REG1.5V
R23 A D1 C
R24 A D2 C
R25 A D3 C
R26 A D4 C
PCI 5V
PCI 3.3V
GND
MT3
MT4
MT5
MT6
MT7
MT8
MT9
MT10
MT11
MT1
J2
J3
J8
C9
C15
C18
C28
C30
C36
U4
U6
U7
TP5
MT14
FD6
C41
PRIMARY