

Columbia University  
Department of Electrical Engineering  
Spring, 2004

**Course:** EECS E4340. Computer Hardware Design.

**Instructor:** Ken Shepard

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**Office:** 1019 CEPSR

**Office hours:** MW 6:45 - 7:45 PM

**TA:** TBD

**Class webpage:** <http://www.cisl.columbia.edu/courses/spring-2004/ee4340/> All course handouts and announcements will be posted on the website.

**Text:** Course “redbook” available in the EE Department office, 1312 Mudd. Unfortunately, there will be a \$18 charge to cover the cost of copying. There will be additional handouts

**Prerequisites:** ELEN E3301 plus ELEN E3910 or CS W3823/W3824.

**Labs:** You will all get computer accounts on the Sun workstations in the VLSI CAD Laboratory (Mudd 1218) and the Linux workstations in the Embedded Systems Lab (Mudd 1235). Your accounts will access both sets of machines and you will have the same home directory in both clusters. We will build and test our hardware in the Computer Hardware Design Lab (Mudd 1211). All rooms will be available with 24-hour badge access for students registered in this course. The

UNIX workstations will all be available for remote `ssh` login. (`telnet` has been disabled for security reasons.) More details can be found on the class homepage.

### References:

None of these books is required reading. We should cover all the material you need in class; however, it may be useful to consult these books at times for a different perspective or more detail. All of the VHDL books are poor (in my opinion); the Bhaskar book noted below is at least short and a little better organized than some of the others.

- Hayes, *Computer Architecture and Organization*, McGraw-Hill.\*
- Lee, *Design of computers and other complex digital devices*, Prentice-Hall, 2000.\*
- Bhaskar, *VHDL Primer*, Prentice-Hall.\*
- Hennessy and Patterson, *Computer Organization: A Quantitative Approach*, Morgan-Kaufmann.
- Prosser and Winkel, *The Art of Digital Design*, Prentice-Hall.\*
- Walkerly, *Digital Design: Principles and Practices*, Prentice-Hall.
- Dally and Poulton, *Digital systems engineering*, Cambridge University Press.
- Salcic and Smailagic, *Digital systems design and prototyping using field-programmable logic*, Kluwer.
- Ercegovic and Lang, *Digital systems and hardware/firmware algorithms*, Wiley.
- Ashenden, *The Designer's Guide to VHDL*, Morgan Kaufmann.

Items denoted with the \* are on reserve in the Engineering library.

**Course goal:** This is a *practical* course, not a theoretical one. My goal is to teach you the art and practice of digital system design by *doing*; as such, most of the focus of the course will be the laboratory and the project, which is also reflected

in the grading (below). The course will include a lot of hands-on experience with industrial design tools and techniques. This is not a circuits course per se, but we will discuss some circuit-related issues as necessary. Students interested in digital *circuit* design should also consider taking ELEN E4321 or ELEN E6930. Those interested in more detailed treatment of computer architecture should consider taking CS W4824.

**Grading:**

- Problem sets: 25% (The five problem sets in the course will be completed individually.)
- Midterm quiz: 25%
- Laboratory sets, final project report, and (oral) presentation: 50 % (A significant fraction of this will be dependent on successfully meeting *intermediate* project milestones; i. e., I want you to stay on schedule.)

**Project:** The centerpiece of this course is the design project. There are two design projects from which to choose (both take advantage of custom printed-circuit boards designed for the course):

- The design of a complete working PDP/8 minicomputer, including interface to memory and a serial port.
- The design of a 100-MHz DDR S-DRAM controller with interface to PCI 64-bit/66 MHz.

Both projects involve detailed register-transfer level design; the second design offers additional challenges in high-frequency board design and I/O bus architecture. The laboratory sets are devoted to the incremental completion of one of these projects.

**Course schedule**

Week 1	Topics	Course introduction. Organization and anatomy of a computer. Introduction to computer architecture.
	Optional reading	Hayes, Chapter 1
Week 2	Topics	Instruction set architectures. Addressing modes. PDP/8 instruction set.
	Reading	Prosser and Winkel, Chapter 7 (blue book)
	Assignment	Problem Set 1. Instruction-set architecture and assembly language programming of the PDP/8
Week 3	Topics	Design hierarchy and processes. Datapath-controller partitioning. ASM charting and state machine design.
	Reading	Prosser and Winkel, Chapters 5 and 6 (blue book)
	Assignment	Tools Tutorial 1. Cadence Composer and VHDL simulation.
Week 4	Topics	Fundamentals of VHDL for register-transfer design
	Optional reading	Bhaskar
	Assignment	Problem Set 2. ASM charting and VHDL modelling

Week 5	Topics	Datapath design and the requirements of the instruction set. Datapath elements: registers, register files, shifter, adders, muxes, multipliers. PDP/8 datapath.
	Reading	Prosser and Winkel, Chapter 8 (blue book)
	Assignment	Laboratory 1. PDP/8 dataflow design.
Week 6	Topics	Control logic design. Hardwired control, microcode, millicode. Testing and validation of hardware.
	Assignment	Laboratory 2. PDP/8 fetch controls.
Week 7	Topics	Memory. Memory hierarchy and memory technology. SRAM and DRAM. Reading datasheets. Types of DRAM; SDRAM, DDR-SDRAM, Rambus.
	Assignment	Laboratory 3A. PDP/8 execution controls. Part 1 Laboratory 3B. DDR S-DRAM controller design.
Week 8	Topics	I/O System Design for the PDP/8. Asynchronous communication discipline UARTs
	Assignment	Laboratory 4A. PDP/8 execution controls. Part 2 Laboratory 4B. PCI interface design.
Week 9	Topics	Logic families and programmable logic. FPGAs. Types of FPGA architectures, programming technology, CAD tools for synthesis and place-and-route
	Assignments	Laboratory 5A. PDP/8 I/O. Laboratory 5B. Interface logic design for DRAM controller. Tools Tutorial 2. Synthesis and FPGA place-and-route tools

Week 10	Topics	Busses. Synchronous and asynchronous protocols. Arbitration schemes, PCI bus as a case example.
	Assignment	Problem Set 3. Busses.
Week 11	Topics	Power, timing, noise issues in digital design. Critical paths, skew, fast paths, asynchronous inputs. Packaging. Power-supply and signal integrity concerns on the board, package, and chip.
	Assignment	Problem Set 4. Power, timing, signal integrity.
Week 12	Topics	High-speed board design. Review of basic transmission line theory. High-speed signalling techniques and standards.
	Assignment	Problem Set 5. High-speed signalling. Laboratory 6. TDR measurement techniques.
Weeks 13, 14		No class. Extensive lab work and final presentation.