

Columbia University
Department of Electrical Engineering
EECS E4340. Laboratory #3B.
DDR S-DRAM Interface
Due: March 31, 2004

This is a complex project and this is the first time that we have done this project. Things are going to be challenging. Please bother me whenever you get stuck and I will help you to move forward.

Please refer to the following documents which can be found on the *Handouts* page on the class website:

- *Xilinx DDR controller reference design.* This is a reference design for a DDR controller that we will be modifying as part of this Lab.
- *DDR S-DRAM datasheet.* We are using the MT46V16M16 part, 4 Meg \times 16 \times 4 banks, operating at 133 MHz.
- *PCI-DDR board schematics.* Please take the time to look at the schematics of the (custom-designed) board that we will be using for this project. At this point, pay particularly attention to the interface between the Virtex-II FPGA (XC2V1000) part that we are using and the DRAM chip.
- *Xilinx data sheets.* These are the datasheets for the Virtex-II FPGA we are using for this project.

Development of the register-transfer-level (RTL) model of the DRAM controller/PCI interface is going to proceed in three parts:

- *Lab 3A.* Modify and become familiar with the DDR controller reference design.
- *Lab 3B.* Become familiar with the Xilinx PCI core and develop a simple testbench to stimulate the core.
- *Lab 3C.* Building interface between DDR controller and PCI core.

After we have finished the RTL model for our design, we will synthesize it to the FPGA and finish debugging on the boards.

In this lab, we are focussing on the first of these three tasks. For your VHDL simulation, we are abandoning the Cadence Composer interface. It is simply too buggy to use now on a design of this complexity; we will work directly with NC-VHDL and files. Things are set-up to work on either the Sun workstations or the Linux workstations. In

/tools2/courses/ee4340/ddr_reference/src,

you will find the source code for the DDR controller design. In

/tools2/courses/ee4340/ddr_reference/func_sim,

you will find the set-up for NC-VHDL simulation. In particular, you will find several important scripts in the

/tools2/courses/ee4340/ddr_reference/func_sim/scripts

directory. *run_analyze* analyzes all the VHDL files for the reference design. *run_elab* runs elaboration (i. e., builds the simulation model from the analyzed VHDL). *run_sim* invokes the simulator on the elaborated model. You will probably want to copy the entire *ddr_reference* directory over to somewhere where you can modify it.

The testbench goes through an initialization sequence in which all banks are precharged, the extended mode register and mode register are loaded, all banks are precharged again, and two auto-refreshes are done. The test bench does some reads and writes to the memory as well.

Please make the following modifications to the design:

- Please modify the controller to work with our memory design; the behavior model for this can be found in

/tools2/courses/ee4340/ddr_reference/src/mt46v16m16.vhd.

- Please remove the *user_int* module, which is not necessary. Have the testbench directly interface to *ddr_ctrl*.
- Add a refresh counter that uses the auto-refresh command to refresh every $t_{refresh}/(t_{period} \times num_rows)$.
- Replace the *CLKDLL* blocks with the *DCM* blocks which are available on the Virtex-II parts. You will need to refer to the datasheets to figure out how to do this.

Please turn in some waveform plots and a very brief write-up describing what you did.