

EOS/ESD Analysis of High-Density Logic Chips

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ABSTRACT

Electrical overstress (EOS) and electrostatic discharge (ESD) are a major cause for field failures in integrated circuits. Effective design of I/O protection circuits is important to achieve overall EOS/ESD reliability. A wide range of CMOS applications is leading to IC chips with different on-chip capacitance values. Using experimental methods combined with device/circuit simulators, we show the important role of chip capacitance on effective I/O protection design.

INTRODUCTION

In this paper we analyze the effect of chip capacitance on the performance of an I/O protection circuit used in advanced CMOS processes. We have experimental results which indicate that the protection levels are strongly influenced by the on-chip capacitance, the stress duration and the protection circuit elements. We have used circuit and device level simulations to study the effect of different on-chip capacitances under EOS and ESD stresses. Based on the simulation and experimental results we provide designers with useful guidelines which account for chip capacitance on the EOS/ESD robustness of the protection circuit.

ADVANCED CMOS I/O PROTECTION CIRCUIT

An effective I/O protection must meet three criteria: (i) efficient clamping action to protect the input buffer gates or the output buffer drains, (ii) occupy minimum area, and (iii) introduce minimum resistance. It should have protection devices to the ground (V_{ss}) and power supply (V_{dd}) to offer protection for ESD stress with respect to both pins. NMOS devices have been used to provide EOS/ESD protection in CMOS technologies[1][2][3]. Figure 1 shows a gate-coupled NMOS (GCNMOS) device designed for a $0.5\mu\text{m}$ silicided CMOS technology. During an ESD event,

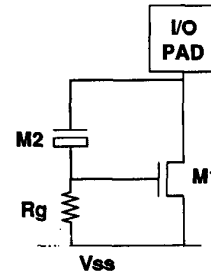


Figure 1: Circuit schematic of a gate-coupled NMOS device showing the booting capacitor M_2 and the gate discharge resistor R_g .

capacitor M_2 pulls the gate high and lowers the *npn* breakdown voltage of M_1 for efficient protection of the input gate oxide. Resistor R_g discharges the gate for normal operation. Components R_g and M_2 are optimized using SPICE [4][5]. It has also been shown that the effectiveness of the GCNMOS is limited for advanced silicided technologies [6].

The GCNMOS protection device concept in advanced CMOS processes has been improved by adding a diode to the V_{dd} line [6][7]. Figure 2(a) shows an advanced protection network for a $0.5\mu\text{m}$ silicided CMOS technology where M_1 is a lateral *npn* (formed by a GCNMOS) and D_1 is a lateral diode to V_{dd} [7]. Diode D_1 , built in an n-well, also forms a vertical *pnp* structure between the pad and V_{ss} , with the base tied to the V_{dd} line (see Fig. 2(b)). During EOS/ESD, the collector current of the *pnp* flows into the substrate which raises the substrate potential. This helps in the uniform turn-on of the parasitic *npn* of M_1 and lowers its trigger voltage. The effectiveness of this substrate interaction is dependent on the layout and both devices should be placed close together to form a compact cell. Since M_1 can protect the gate oxide as well as trigger before an output buffer device, no additional series resistance between the protection device and the I/O devices is required. Thus the scheme in Fig. 2(a) meets all the three requirements above.

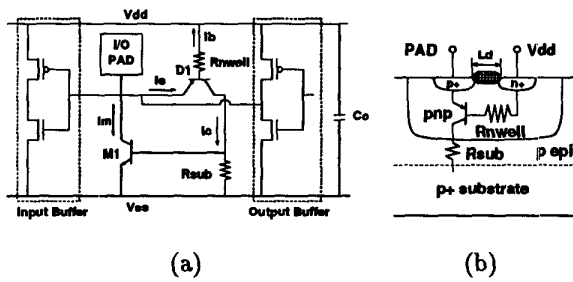


Figure 2: (a).Circuit schematic of the I/O protection circuit showing the lateral *pn* diode to V_{dd} and chip capacitance between V_{dd} and V_{ss} . Also shown are the currents through the *npn* (I_m) and *pnp* devices (I_c , I_b and I_c). (b) Cross-section of the lateral n-well *pn* diode showing the parasitic *pnp*.

The diode *D1* should be designed with minimum length to minimize its series resistance and effectively conduct the stress current away from the PMOS in the output buffer. During the initial stress event the chip capacitance (C_c in Fig. 2(a)) is expected to play an important role. For logic chips C_c can vary from a hundred pF (standard logic) to tens of nF (large microprocessors). In this work, we study the effect of C_c and optimize the protection network for overall EOS/ESD performance.

EXPERIMENTAL RESULTS

Under ESD stresses ($< 1\mu s$), the protection device M1 turns-on uniformly and provides full protection. Experimental data shows that the *npn* turns on efficiently for C_c of at least 1nF but is ineffective when C_c is between 1pF and 100pF (see Fig. 3). However, beyond 1nF, C_c has no impact on ESD but has an influence on EOS as described below.

The current-to-failure (I_f) versus time-to-failure (t_f) curve gives information on the overall EOS/ESD robustness of a protection circuit [8]. The effect of the chip capacitance was experimentally analyzed using this method. The I_f - t_f curves for the protection circuit in Fig. 2(a) are shown in Fig. 4 for chip capacitance values of 3nF and 100nF.

The failure current (I_f) is higher for a larger chip capacitance in the EOS regime ($> 1\mu s$). However, the improvement is limited by the current profile of the stand-alone

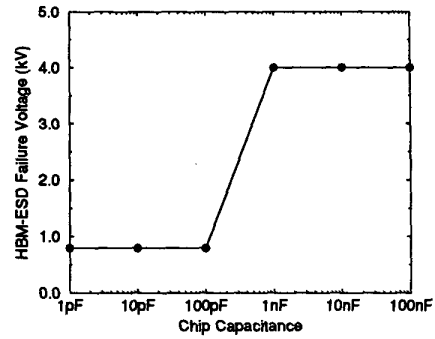


Figure 3: Variation of the Human Body Model (HBM) ESD failure voltage with the chip capacitance.

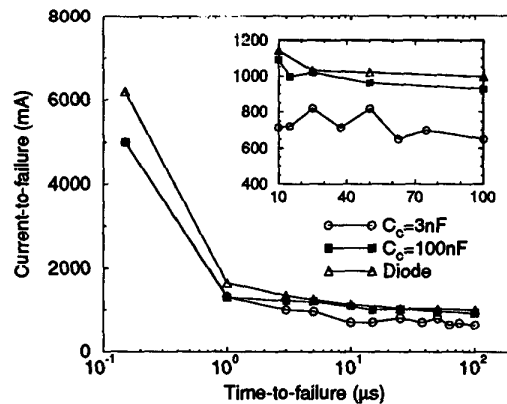


Figure 4: Variation of failure current (I_f) with time-to-failure (t_f) for the diode compared with those for the protection circuit with $C_c=3nF$ and 100nF. The inset shows a magnified plot of the same profiles for the EOS regime.

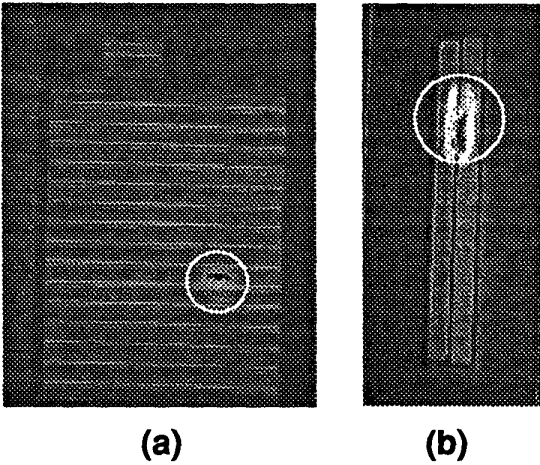


Figure 5: SEMs showing (a) NMOS failure under ESD and (b) diode failure under EOS.

pn diode curve also shown in Fig. 4. These observations were confirmed by failure analysis where *M1* failed under ESD stress and *D1* failed under EOS (see Fig. 5). The experimental results reveal that for maximum protection both *M1* and *D1* in Fig. 2(a) must be fully optimized. In the following sections we provide analytical equations and 2D device and circuit simulations to describe EOS stress effects. These are then combined with the experimental results to provide useful design guidelines.

MODELING THE EFFECT OF CHIP CAPACITANCE

In this section we present a set of equations which describe the operation of the protection circuit under EOS/ESD. Initially, the forward biased diode conducts the stress current to charge up the V_{dd} line. An EOS/ESD stress can be represented as a square pulse [9] [10] using different pulse widths. The time taken to charge the capacitance (C_c) to a voltage (V_c) with a current pulse having a peak current (I_p) can be obtained from the capacitance charge equation as

$$\int_0^{t_c} dt = C_c \int_0^{V_c} \frac{dV}{I(t)} \approx C_c \frac{V_c}{I_p}. \quad (1)$$

Since the diode has a finite on-resistance (R_d) during forward conduction, the pad voltage is given by

$$V_{pad} = V_{be} + I_b R_d + V_c \quad (2)$$

where V_{be} is the forward voltage drop across the emitter-base junction of the *pn* and I_b is the base current which charges the capacitor. The capacitor continues charging-up till the pad voltage reaches the trigger voltage (V_{trig}) of *M1*. Hence the total charging time (t_c), which is related to the diode conduction time, can be given by (from (1) and (2)),

$$t_c = \frac{C_c}{I_b} (V_{trig} - I_b R_d - V_{be}) \quad (3)$$

We now need to relate the base current (I_b) to the pad current (I_{pad}) through the gain (β) of the parasitic *pn* device. The gain of the vertical *pn* can be obtained from two sets of measurements described below. In Fig. 6, we show a section of the protection circuit which conducts during the charge-up phase. We first measure the pulsed I-V characteristic of the circuit with the V_{dd} line grounded and the substrate left floating. This gives us the forward charac-

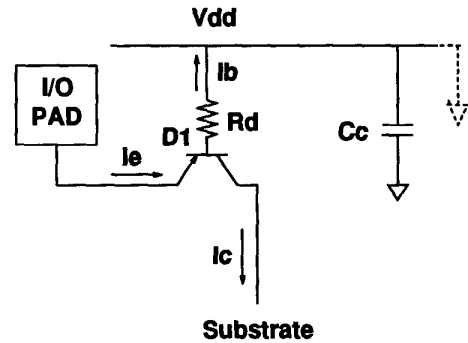


Figure 6: Section of the protection circuit involved in charging the V_{dd} line during EOS.

teristics of the lateral *pn* diode as shown in Fig. 7. The on-resistance R_d can be measured from the curve which in this case is around 4.5Ω . The next measurement involves hooking a large external capacitor (100nF in this example) between the V_{dd} line and V_{ss} with the substrate grounded. The same pulse width is used to measure the pad's I-V characteristics. The gain of the vertical *pn* can be obtained by measuring the difference in the two voltages for a given pad current (within the linear charge-up phase) using

$$\beta = \frac{I_{pad}}{I_b} - 1 = \frac{I_{pad} t_{pw}}{C_c \Delta V} - 1 \quad (4)$$

where t_{pw} is the pulse width used for the measurements and ΔV is obtained as shown in Fig. 7. A sample pulse

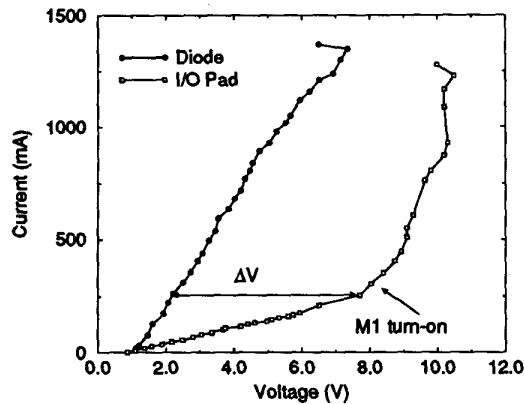


Figure 7: Pulsed I-V characteristics for the *pn* diode and I/O pad for $3\mu\text{s}$ stress pulses.

measurement is shown in Fig. 8 which clearly indicates the linear charge-up phase. This technique was used to construct a plot of the *pn* gain as a function of the emitter (pad) current in Fig. 9. Hence we can relate the charge-up

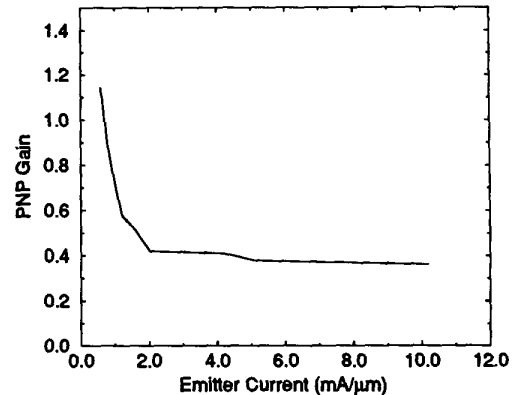


Figure 9: Measured gain of the vertical *pn* transistor in the $0.5\mu\text{m}$ CMOS process. At high stress levels the gain is low and most of the current flows into the base of the *pn*.

time (t_c) to the pad current (I_{pad}) as

$$t_c = \frac{C_c}{I_{pad}} (\beta + 1) (V_{trig} - \frac{I_{pad}}{\beta + 1} R_d - V_{be}) \quad (5)$$

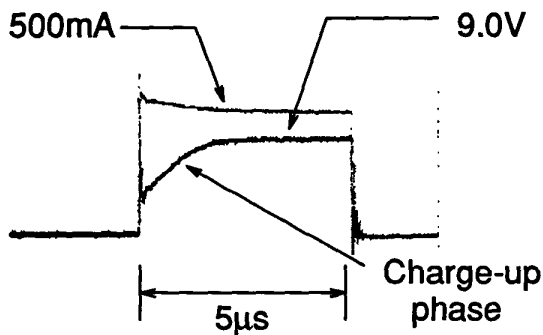


Figure 8: Measured current and voltage waveforms for the I/O protection circuit under a $5\mu\text{s}$ current stress of 500mA. Note that the charge-up time (t_c) is almost $1.5\mu\text{s}$.

SIMULATION RESULTS

The circuit simulator iETSIM [11] has been updated with the MOS snapback model [12]. We used this simulator to analyze the protection circuit for different values of C_c and for different stress levels (e.g., see Fig. 10). The gain of the *pn* is low at high current levels (see Fig. 9) and most of the stress current appears as the base current to charge C_c . Under ESD stress the capacitance charges up quickly to the trigger voltage of M1 and prevents failure of the diode which has a higher I_f . However, under EOS, if the charging time (t_c) is greater than the diode failure time for a given stress current, the diode fails prematurely. Hence, the diode can be the weak link under EOS. The diode, if not properly designed, can be weak for small chips as well. We used two-dimensional electrothermal simulations to study the failure mode of the diode under EOS [13][14]. Figure 11 shows the response of the

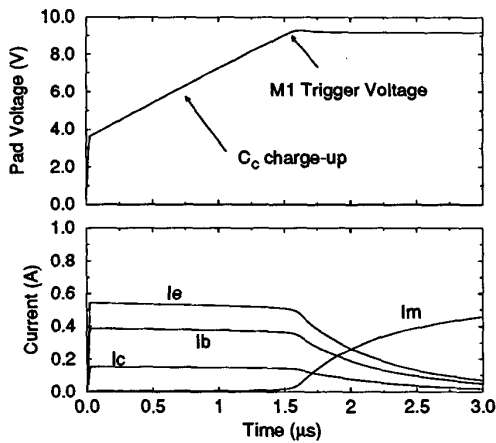


Figure 10: Circuit-level simulation for 500mA stress current with a 100nF chip capacitance. Note that the stress current is conducted by *D1* for over 1.5 μ s (I_e , I_b and I_c), while *M1* conducts the current after 3 μ s (I_m).

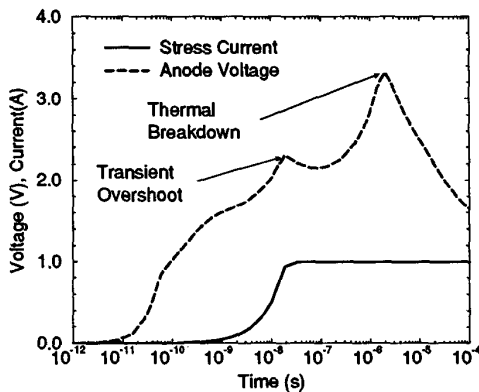


Figure 11: 2D Electrothermal device simulation results for a lateral *pn* diode. Note that the device ($W=50\mu\text{m}$) fails at around 1 μ s for a 1A (20mA/*mum*) stress level.

diode when subjected to a 20mA/ μm stress with appropriate thermal boundary conditions. As the temperature rises in the n-well the pad voltage increases due to mobility degradation. As shown in the figure, as the temperature rises further, the n-well becomes intrinsic and the pad voltage drops after around 1 μ s. This indicates the onset of thermal runaway and catastrophic device failure. This simulation reveals that the diode is susceptible to thermal failure and validates our observation of diode failures under EOS. The thermal failure current versus failure time for diodes with two widths is compared in Fig. 12 with the charge-up profile obtained from iETSIM simulations. It can be seen that the diode must be at least 50 μm wide to prevent its premature failure during the charge-up phase. The optimal design ensures that the I_f - t_f curve of the diode lies above the charge-up profile for the full range of EOS/ESD stress events.

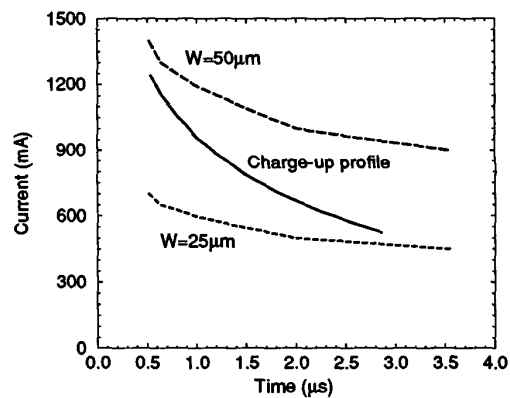


Figure 12: Simulated thermal failure current versus time-to-failure for a diode with two widths compared with the charge-up profile for $C_c=100\text{nF}$. The charge-up profile is a plot of the current flowing into the diode versus the time needed to fully turn-on *M1*.

CONCLUSIONS

The EOS/ESD design issues for an advanced CMOS protection scheme were analyzed using experimental methods and circuit/device level simulations. From this study we conclude that *M1* and *D1* in Fig. 2(a) along with the chip capacitance (C_c) play an important role in defining the

overall EOS/ESD reliability. When $M1$ ($500\mu\text{m}$) and $D1$ ($50\mu\text{m}$) are placed together in an optimum layout, greater than 4 kV HBM-ESD performance is obtained as long as a minimum chip capacitance of 1nF is present. However, for the longer duration EOS pulses, the capacitance has a direct impact. For chips with capacitance of only a few nF, additional thin oxide capacitors can be added between V_{dd} and V_{ss} to boost their failure current to the same level as chips with larger capacitance. This work has shown that optimum layout of the protection device cell with its individual components and the interactive effect of the chip capacitance are critical to obtain good EOS/ESD reliability for IC chips.

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