A 2–1600-MHz CMOS Clock Recovery PLL with Low-$V_{dd}$ Capability

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Abstract—A general-purpose phase-locked loop (PLL) with programmable bit rates is presented demonstrating that large frequency tuning range, large power supply range, and low jitter can be achieved simultaneously. The clock recovery architecture uses phase selection for automatic initial frequency capture. The large period jitter of conventional phase selection is eliminated through feedback phase selection. Digital control sequencing of the feedback enables accurate phase interpolation without the traditional need of analog circuitry. Circuit techniques enabling low-$V_{dd}$ operation of a PLL with differential delay stages are presented. Measurements show a PLL frequency range of 1–200 MHz at $V_{dd} = 1.2$ V linearly increasing to 2–1600 MHz at $V_{dd} = 2.5$ V, achieved in a standard process technology without low threshold voltage devices. Correct operation has been verified down to $V_{dd} = 0.9$ V, but the lower limit of differential operation with improved supply-noise rejection is estimated to be 1.1 V.

Index Terms—Frequency locked loops, frequency synthesizers, phase comparators, phase jitter, phase locked loops, phase noise, synchronization.

I. INTRODUCTION

THE continuing scaling of CMOS process technologies enables a higher degree of integration, reducing cost. This fact, combined with the ever shrinking time to market, indicates that designs based on flexible modules and macro-cells have great advantages. In clock recovery applications, flexibility means, for example, programmable bit rates requiring a phase-locked loop (PLL) with robust operation over a wide frequency range. Increased integration also implies that the analog portions of the PLL (mainly the voltage-controlled oscillator [VCO]) should have good power-supply rejection to achieve low jitter in the presence of large supply noise caused by digital circuitry.

Another trend is low-power design using reduced $V_{dd}$. This reduces the headroom available for analog design, causing integration problems for mixed-mode circuits [1]. Furthermore, in applications where power consumption is a more critical design goal than compute power, $V_{dd}$ is not scaled as aggressively as $V_{dd}$ to avoid leakage currents in OFF devices, which aggravates the headroom problem. For mixed-mode circuits with significant analog circuitry, dual-$V_{dd}$ and/or dual-$V_{dd}$ processing combined with a dc/dc converter [2] is a viable solution. However, for circuits dominated by digital logic, it is difficult to justify the additional fabrication steps required for these solutions. A common case of the latter mixed-mode design is a large digital circuit incorporating a PLL-based clock generator with low-jitter requirements, which is the most common mixed-mode design today. Digital style PLL’s have been suggested, e.g., [3], but these cannot compete with the supply-noise rejection of differential analog circuitry.

A clock recovery PLL architecture suitable for programmable bit rates is developed in Sections II and III with emphasis on jitter reduction. Sections IV–VI present PLL circuit techniques that use the noise resistant differential pair but avoid other “expensive” (in terms of headroom) analog circuitry, such that low-$V_{dd}$ operation is enabled in a standard digital CMOS process without the need of low-threshold devices.

II. LOW-JITTER PHASE-SELECTING CLOCK RECOVERY

A basic PLL for clock recovery is shown in Fig. 1(a). In most CMOS implementations, the VCO must have a tuning range covering more than ±50% of the target frequency to guarantee high yield over large process variations. This large frequency range requires special techniques for initial frequency locking since there exists no phase detector for nonreturn-to-zero (NRZ) data that operates reliably with large initial frequency offset. Available techniques include frequency sweeping [4], using a replica VCO matched to the clock generating VCO [5], or initially locking the PLL to a reference frequency with a frequency detector before switching to the input data and locking with a phase detector [6].

One common technique requiring no special initialization is shown in Fig. 1(b). This dual-loop PLL can be traced back to [7], which was based on a delay-locked loop (DLL). The multiple-output VCO in Loop A in Fig. 1(b) generates a number of equally spaced clock phases at a frequency of $N \cdot f_{ref}$. This loop can have a large frequency tuning range since it is locked with a phase frequency detector (PFD). Clock recovery is performed by Loop B that generates the recovered clock by selecting the clock phase from Loop A that is best aligned with the incoming data. If there is a frequency offset between $N \cdot f_{ref}$ and the incoming data, an appropriate clock can still be generated by changing the Ctrl signal to select a different phase over time.

Frequency initialization is automatically achieved by selecting appropriate $f_{ref}$ and $N$ for the expected data rate. Most communication systems have a frequency tolerance of a few hundred parts per million (ppm), eliminating any need for a frequency detector in Loop B. The decoupling of the VCO loop from the data recovery loop enables independent selection of bandwidth in those two loops. This allows a large bandwidth in...
Fig. 1. Clock recovery PLL’s. (a) Standard, (b) phase selection, and (c) feedback phase selection. ChP+F denotes charge pump + loop filter.

Loop A to suppress VCO jitter [4], for example, jitter induced by power-supply noise. At the same time, a low bandwidth can be used in Loop B to reduce jitter transfer. This cannot be achieved by the PLL in Fig. 1(a), which has a single loop with conflicting design goals regarding loop bandwidth.

A disadvantage of a phase-selecting PLL is that the phase step that is generated when the Ctrl signal in Fig. 1(b) switches to a new clock phase. This phase switching leads to large cycle-to-cycle jitter (greater than or equal to the phase spacing) that can actually dominate the peak-to-peak jitter. By increasing the number of phases, the phase spacing will be smaller with less jitter. More phases can be generated by having more delay stages in the VCO, but this limits the speed. An alternative is phase interpolation that enables a large number of phases without degrading the VCO speed [8], [9]. However, interpolators add analog circuitry to the design and are prone to mismatch, which in the worst case can lead to nonmonotonic phase spacing.

A proposed remedy for the jitter due to phase steps is shown in Fig. 1(c). Instead of selecting a clock phase feeding the sampling flip-flop and the phase detector, the feedback clock in Loop A is selected from the multiple VCO phases. When Loop B detects a misalignment of the incoming data and the VCO output clock, the Ctrl signal is changed to select a different phase for the feedback clock. This will cause a phase change in the divided clock feeding the PFD such that the charge pump will alter the VCO control voltage stored in the loop filter. Therefore, sudden phase steps generated by the clock recovery logic will be smoothed by the filter of Loop A, causing the VCO clock to slowly drift toward the correct phase with a rate of change determined by the bandwidth of Loop A. In a 622-MHz application with a division ratio of $N = 8$ and a bandwidth of Loop A equal to one-tenth of $f_{ref}$, it will take approximately $8 \times 10 = 80$ clock cycles to complete a phase switch. The jitter caused by a phase step in the structure in Fig. 1(c) is therefore spread out over 80 clock cycles, significantly reducing the jitter compared to Fig. 1(b). Feedback phase selection has previously been applied to fractional-$N$ frequency synthesizers for other purposes [10], [11].

III. AVERAGING PHASE INTERPOLATION

The smoothing effect of the loop filter can also be used for phase interpolation. If the Ctrl signal in Fig. 1(c) alternates between two different clock phases every second cycle of the reference clock, the result will be a VCO clock phase corresponding to the average of the two selected phases. In the test chip, four levels of averaging phase interpolation were implemented by circulating through four clock cycles and in each clock cycle selecting phase $\phi_m$ or $\phi_{m+1}$ as the feedback clock. A quarter phase interpolation generating $\phi_{m+0.25}$ is then achieved by selecting $\phi_m$ for three consecutive clock cycles, then selecting $\phi_{m+1}$ for the fourth cycle and repeating this sequence.

The architecture in Fig. 1(c) lends itself naturally to combining both averaging phase interpolation and standard current-mode interpolation. A test chip was built in a 0.25-µm, 2.5-V digital CMOS process to evaluate the jitter performance of the phase selection architecture. A block diagram of the implemented VCO and phase control circuitry is shown in Fig. 2. The phase select control code at the input consists of seven bits, of which two are directly fed to a finite state machine (FSM) that generates control signals for realizing the averaging interpolation. The remaining five bits of the control code represent $\phi_m$, from which the code for $\phi_{m+1}$ is generated by adding one. The FSM controls Mux1 to select one of the codes representing $\phi_m$ and $\phi_{m+1}$ in a four clock period repetitive cycle, as described above. The five bits at the output of Mux1 are split into three bits coarse select and two bits fine select. The three coarse bits select two neighboring phases from a four-stage differential VCO having eight evenly spaced output phases and send these two phases to a current-mode interpolator. Mux2/Mux3 in Fig. 2 receive one coarse bit each, and the third coarse bit is used to conditionally invert the output signals. The interpolator is similar to the Type-I circuit in [9] and is controlled by a four-bit temperature code derived from the two fine select bits. Both the current-mode interpolation and the averaging phase interpolation are programmable in the test chip and can be disabled. The two complementary multiplexers at the output...
of the VCO/interpolator (Mux4/Mux5) allow the chip to be configured for the scheme in either Fig 1(b) or (c), enabling a performance comparison.

Freezing the 7-bit phase select control code to a fixed phase gives a measured output period jitter\(^1\) of 7.6 ps rms when running the VCO at 500 MHz, as shown in Fig. 3(a). This is the jitter inherent in the VCO and the output buffers. Configuring the chip for the standard phase selecting scheme in Fig. 1(b) with 32 clock phases (4\(\times\) interpolation) gives the jitter in Fig. 3(b), revealing a long tail in the histogram caused by a frequency offset of 1200 ppm between the incoming data and \(N \cdot f_{\text{ref}}\). The phase spacing is 2 ns/32 = 62.5 ps such that we can expect a second peak in the histogram 62.5 ps away from the main peak, which is confirmed by the shape of the histogram. As shown by the inset, this peak is slightly off its ideal position and is smeared out due to the nonideal ac behavior of the current-mode interpolator.

Feedback phase selection with 4\(\times\) current-mode interpolation eliminates the long tail in the histogram, bringing the period jitter down to 7.9 ps rms, as shown in Fig. 3(c). This indicates that the jitter is completely dominated by the VCO jitter, and nearly all of the phase-switching jitter caused by digital clock recovery can be eliminated. Fig. 3(d) shows the period jitter histogram obtained when the current-mode interpolators are disabled and 4\(\times\) averaging phase interpolation is used instead. Its similarity to the result in Fig. 3(c) proves that the same low jitter and the same number of discrete clock phases (32) can be achieved without the analog interpolation circuitry.

Enabling both the current-mode interpolator and the averaging phase interpolation gives a total of 128 selectable clock phases. The graph in Fig. 4 shows the phase shift as a function of the phase select control code when the period of the VCO is 1 ns. The expected phase step is 21 ps, whereas the largest measured step is 21 ps, resulting in a differential nonlinearity (DNL) of 1.7 bits. The differential VCO makes the phase curve near-symmetric around the midpoint, suggesting that the integral nonlinearity (INL) of 94 ps is mainly due to delay mismatch in the VCO. The main contributing factor to this mismatch is unbalanced parasitic wiring capacitors that are difficult to match without incurring speed penalty. If Loop B is a first-order loop or a well-damped second-order loop, the feedback in Loop B will automatically select the best fit phase select code, reducing the impact of INL. The maximum phase deviation in a clock recovery application is then the DNL added to the VCO jitter.

In addition to jitter reduction and phase interpolation, feedback phase selection also has other advantages when combined with other architectures. Using feedback instead of feedforward phase selection reduces circuit complexity, thereby eliminating the need for good matching in an analog-style interpolator [12] and a high-speed parallel sampling structure [13].

IV. VCO

Recently, low-noise VCO’s utilizing high-swing complimentary signals have been presented (e.g., [14] and [15]).
Good 1/f noise performance has been shown, but their power-supply noise rejection is inferior to that of the standard analog differential pair since they lack a high-impedance source, making the delay depend on Vdd. Therefore, the analog style differential pair is preferable in applications where power-supply noise is the main source of oscillator jitter. When a differential pair with resistor loads is used as a delay cell in a VCO, the frequency is regulated by changing the tail current as implemented by the Vref control voltage in Fig. 5(a). To achieve a large frequency tuning range, it is desirable that the output swing and common mode do not change significantly with frequency. Often the replica-bias scheme in Fig. 5(a) is employed, which relies on good matching between a replica of the delay stage (devices Mr1–Mr3) and the VCO delay stages to set the VCO output swing from Vref to Vdd, giving a known common mode and swing independent of the speed-regulating current. A disadvantage of this technique is that the PMOS load (Mr3) will operate as a current source at low frequencies, introducing high gain in the replica feedback loop. To prevent instability, a large compensation capacitor is required, which introduces another pole in the PLL, leading to more intricate design. Furthermore, the amplifier in the replica bias loop requires additional headroom, thereby prohibiting low-Vdd operation.

Fig. 5(b) shows a structure that achieves the good power-supply noise rejection of the analog differential pair, at the same time enabling low-Vdd operation. The PMOS diodes are used for clamping the output voltage to a minimum level of Vdd - |Vtp|, giving a fixed common mode and swing without the need for a replica bias circuit. This makes the VCO suitable for a wide range of operating frequencies and supply voltages. To guarantee clamping action, the NMOS tail current (I_T) must be larger than the current through the controlled PMOS load (I_L). Furthermore, a proposed design goal for low oscillator noise suggests that the rise and fall times of the output nodes should be made equal [16]. This is achieved by reflecting half of I_T to each of the controlled PMOS loads by the current mirror formed by devices Md1–Md3. Assuming that Md4 recently turned on, “node a” will be discharged by a current of I_T - I_L = I_T - I_T/2 = I_T/2. At the same time, the complementary output node is pulled to Vdd by a current equal to I_L = I_T/2, indicating equal rise and fall times. A disadvantage of this oscillator is the additional parasitic capacitance of the diodes, which makes the maximum operating frequency lower than that of the replica bias structure. The additional gate capacitance of the diode loads can be eliminated by using NMOS diodes [17].

The minimum supply voltage for the VCO is Vdd = max(V_in, Vtp), which has been verified by measurements down to Vdd = 0.9 V. However, at this value of Vdd, the VCO is no longer differential. An estimate of the minimum Vdd for differential operation can be derived from the simulated VCO waveforms in Fig. 6. The VCO output swings from Vdd down to approximately Vdd - |Vtp|. For differential operation, it is required that both NMOS devices in the differential pair (Md4, Md5) are turned ON at the crossover point of the waveforms. Assuming a VDsat drop over the current source device Md6 leads to a minimum input voltage of VDsat + Vtp. At the lowest limit of Vdd, this input voltage is Vdd - |Vtp|/2 generated by the previous stage in the oscillator, indicating a minimum Vdd of V_in + |Vtp|/2 + VDsat. Measurements determined V_in and |Vtp| to be 0.53 and 0.85 V, respectively, indicating a minimum Vdd of about 1.1 V assuming a VDsat of 0.1 V. Note that this is a theoretical number, since the differential operation of the VCO has zero tuning range at this value of Vdd. Good power-supply rejection can also be achieved by the regulated-supply structure in [18]. However, the requirement of a large decoupling capacitor generates contradicting design goals on PLL bandwidth.

V. CHARGE PUMP

A. Bandwidth and Peaking Compensation

To reduce peak-to-peak jitter due to VCO noise, it is advantageous to keep as high a PLL bandwidth as possible. Traditional worst case design would keep the PLL bandwidth and damping factor sufficiently far away from stability limits under all variations of the input reference frequency, the
manufacturing process, and the division ratio in the feedback path \( N \). The concept of self-biasing introduced in [19] simplifies the design by eliminating process variations and the input reference frequency from the stability constraints. However, the PLL bandwidth is still a function of \( N \), so that maximum noise suppression can only be achieved for a fixed \( N \). In programmable applications, \( N \) can vary by more than an order of magnitude, indicating that the variation in stability constraint can be dominated by \( N \) instead of process variations, as shown by the stability limit of a charge-pump PLL [20]

\[
    f_{\text{ref}} \geq \frac{K_o \cdot I_p \cdot R}{N \cdot A}\n\]

where \( f_{\text{ref}} \) is the input reference frequency (or effectively the sampling rate of the phase detector), \( K_o \) is the VCO gain, \( I_p \) is the charge-pump current, and \( R \) is the loop filter resistance. Other PLL design parameters, such as bandwidth and damping factor, also change with \( N \). Compensating loop parameters for changes in \( N \) guarantees that the PLL is always operating with maximum bandwidth and fixed damping factor without endangering stability. This can be done by setting the charge pump current to

\[
    I_p = N \cdot I_{\text{ref}}\n\]

where \( I_{\text{ref}} \) is a fixed reference current. This is realized by the current multiplier in Fig. 7, which generates the charge-pump current \( I_p \) by letting the individual bits of \( N \) control binary weighted current sources.

The simulated jitter transfer function of a standard PLL in Fig. 8(a) demonstrates the change of loop parameters as \( N \) is altered. The damping factor is intentionally set low to show its dependence on \( N \). The measured jitter transfer function of Loop A in Fig. 8(b) shows the desired independence of \( N \). The slight deviation of the curves is caused by transistor mismatch in the current multiplier.

**B. Charge Sharing**

A common problem of many charge pumps is charge sharing. For the charge pump in Fig. 9(a) (Type A), charge sharing is caused by the parasitic capacitance in nodes \( pcs \) and \( ncs \) [21]. When \( I_{\text{Up}} \) is active, node \( pcs \) is charged to \( V_{ddl} \). When deactivating \( I_{\text{Up}} \), some of the charge stored in node \( pcs \) will leak through the current source device. Since the parasitics of nodes \( ncs \) and \( pcs \) can never be matched, this will lead to a static phase offset, as shown in Fig. 10(a). This is the transfer function of a phase-frequency detector followed by a Type A charge pump. The two transistors \( Mp \) and \( Mn \) in the Type B charge pump in Fig. 9(b) will remove the charge from the nodes \( pcs \) and \( ncs \) when \( Up \) and \( Down \) are deactivated [22]. This leads to a large reduction in the phase offset, as shown in Fig. 10(a).

For this application, static phase offset in Loop A is not critical. However, when analyzing the cause of phase offset, a source of increased jitter is revealed. Fig. 10(b) indicates that the leakage from node \( pcs \) is larger than that from \( ncs \). When the PLL is locked, the leakage mismatch is compensated for by activating \( I_{\text{Down}} \) earlier than \( I_{\text{Up}} \) giving a phase offset. Since the compensation charge is applied in the early portion of the charge-pump activation time, it will cause voltage ripple on
Fig. 10. Characteristics of the Type A and B charge pumps. (a) Transfer function of PFD followed by charge pump. (b) Simulated $I_{\text{Up}}$ and $I_{\text{Down}}$ when net output charge is zero.

the loop filter, leading to phase jitter at the VCO output. The charge removal transistors $M_n$ and $M_P$ in Fig. 9(b) eliminate the current tails resulting in a well-balanced $U_p$ and $D_n$ activation time such that $I_{\text{Up}}$ and $I_{\text{Down}}$ cancel each other, reducing the loop filter ripple. A further advantage of the Type B charge pump is reduced $1/f$ noise in the current source transistors achieved by periodically resetting their $V_{GS}$ to below $0$ V [23], [24].

A limitation of the Type B charge pump is a reduced dynamic range of the VCO control voltage ($V_{\text{VCO}}$). If $V_{\text{VCO}}$ is less than $V_{\text{GDN}} - V_{\text{TR}}$, there will be a current flowing through the $M_P$ device to the output when the $D_n$ control is inactive. When NMOS devices are used for speed-regulating the VCO, $V_{\text{VCO}}$ will never drop below $V_{\text{TR}}$, constraining $V_{\text{GDN}}$ to be less than $2V_{\text{TR}}$, which can easily be fulfilled. However, the charge pump works only up to an output voltage of $V_{\text{VCO}} < V_{\text{GDN}} + |V_{\text{TP}}|$, limiting the upper tuning range of the VCO. However, the charge pump in Fig. 9(a) has the same upper voltage limit. Mismatch in $I_{\text{Up}}$ and $I_{\text{Down}}$ is a similar source of jitter as charge sharing described above. For low jitter, it is essential to have good matching, implying that the devices controlled by $V_{\text{GDN}} / V_{\text{GDP}}$ should be saturated. Again, this requires $V_{\text{VCO}} < V_{\text{GDN}} + |V_{\text{TP}}|$.

Charge removal can also be done by ac coupling [18], but this requires careful timing of the control signals in the charge pump. The solution to charge sharing in [21] is less suitable for low-$V_{DD}$ applications due to the common-mode restrictions on the differential amplifier.

VI. LOOP FILTER

The most common PLL loop filter is the simple RC circuit in Fig. 11(a). Common design options for the resistor are poly or the channel resistance of an MOS transistor. For high resistance values, an MOS device is most attractive. However, it has a disadvantage at low $V_{DD}$ if implemented with the straightforward configuration of Fig. 11(b). For a nominal $V_{DD}$ of $2.5$ V, the effective resistance of the transmission gate is nearly independent of the VCO control voltage ($V_{\text{VCO}}$). However, the resistance becomes strongly dependent on $V_{\text{VCO}}$ for low $V_{DD}$. For $V_{DD} = V_{\text{TN}} + |V_{\text{TP}}|$, the resistance goes to infinity for some values of $V_{\text{VCO}}$ [25], [26]. Exchanging the position of the transmission gate resistor and the MOS capacitor as in Fig. 11(c) will make $V_{GS}$ and the resistance of the NMOS device independent of $V_{\text{VCO}}$. The resistance still varies with $V_{DD}$, but the variation is much less than for the previous configuration.

Since the capacitor $C$ in Fig. 11(c) is a “floating” capacitor, it must be implemented with a PMOS device. When the VCO control voltage approaches $|V_{\text{TP}}|$, the MOS device is between inversion and depletion, where its capacitance value is voltage dependent, as shown in Fig. 12. By altering the gate and source/drain connections of the PMOS as shown in Fig. 11(d), it will operate in accumulation where the capacitance value is less voltage dependent, as shown for $V_{\text{VCO}} > 0.5$ V in Fig. 12. To avoid strong power-supply noise injection, the well must be connected to the same node as source and drain, as shown in Fig. 11(d). The corresponding filter model is
shown in Fig. 11(e), where $C_3$ is the parasitic well-to-substrate capacitance of the MOS capacitor. This filter has an impedance of

$$Z_e = \frac{R \cdot (1 + C/C_3) + 1/sC_3}{sRC + C/C_3}$$

which is a close approximation to the impedance of the original filter in Fig. 11(a), given as

$$Z_a = \frac{R \cdot C/C_3 + 1/sC_3}{sRC + 1 + C/C_3}$$

when $C \gg C_3$, as is common design practice [20].

VII. PHASE-FREQUENCY DETECTOR

Phase detectors may exhibit a dead zone, resulting in enlarged jitter. A common design technique to avoid a dead zone is to make sure that both Up and Down output signals are fully activated before shutting them both off. This is implemented by generating a reset signal with an AND operation of Up and Down output and introducing a delay before feeding back this signal to reset the phase detector. It is this reset delay that causes the simultaneous $I_{Up}$ and $I_{Down}$ in Fig. 10(b). If the charge sharing in the charge pump is not perfectly cancelled or if there is a mismatch of $I_{Up}$ and $I_{Down}$ there will always be some current compensation, leading to phase offset and loop filter ripple, as discussed in Section V. A longer reset delay results in a longer period during which the VCO is running at a different frequency due to the compensation current. Therefore, the reset delay should be minimized under the constraint that it has to be longer than the response time of the PFD with some additional design margin to avoid a dead zone.

A PFD with low logic depth is shown in Fig. 13, including details of the Up section. Its operation is easiest to analyze by assuming an initial state of $R = V = U_p = D_{up} = 0$. This implies that $Rstb = u1 = 1, u2 = 0$ and that $u3$ is precharged high. A rising edge on $R$ discharges $u3$ and sets $U_p = 1$ without changing the state of the RS flip-flop. The internal weak feedback in the $U_p$ path will assure that $U_p$ is kept active even if $R$ falls. At the next rising edge on $V$, $D_{down}$ is activated, which sets $Rstb = 0$. This triggers the RS flip-flop to precharge $u3$ high, which shuts off $U_p$ and, at the same time, $D_{down}$ is deactivated in a similar way.

In summary, a positive edge on $R$ sets $U_p = 1$, which is reset by the next positive edge on $V$. This behavior is identical to the two classical PFD’s implemented by either four RS flip-flops or two resettable D—flip-flops. The precharged gate and the shorter logic depth of this implementation make the delay shorter than for the standard PFD’s. This allows a smaller delay in the reset path for eliminating the dead zone, such that loop filter ripple will be reduced and generate less noise. An additional benefit of low logic depth is a reduction in phase detector jitter caused by power-supply-dependent delays and device noise.

The reset delay of this PFD can be further reduced by letting the signal $Rstb$ directly reset the precharged gate simultaneously as the RS flip-flop is reset. This technique was not adopted in order to keep a conservative design, guaranteeing operation with no dead zone. Similar precharged gates have previously been used in PFD designs [27]–[29].

VIII. FREQUENCY DIVIDER

To enable high flexibility, the frequency divider in Fig. 2 is a fully programmable $(2 \leq N \leq 65)$ divider. The structure in [30] based on a clock-gated dual-modulus prescaler followed by a counter was chosen to achieve high speed at low supply voltages. The divider was realized in standard static CMOS logic, reaching a maximum operating frequency of 800 MHz in simulations of worst case slow process variation at $Vdd = 1.6$ V and $T = 125^\circ$C. This exceeded the simulated speed limit of the VCO. The potential startup deadlock in [30] was eliminated by logic that prohibits two consecutive clock pulse removals.

IX. PLL OPERATING RANGE AND JITTER

The maximum operating frequency of the PLL measured at room temperature is plotted in Fig. 14 as function of $Vdd$. Simulations indicate that the speed is limited by the VCO. A minimum $Vdd$ of 0.9 V agrees well with the measured $|V_{th}| = 0.85$ V. At low power-supply voltages, the speed cannot compare with high-end circuits using standard Vdd. However, the operating frequency range exceeds that of low-voltage circuit implementations [2], [3], [25], [26]. The maximum speed also compares favorably with another low-voltage PLL based on a low-threshold process [18].

With a PLL bandwidth of 2 MHz, the tracking jitter is 5.2 ps rms at 1200 MHz, as shown in Fig. 15(a). This measurement represents the standard deviation of the delay between a
triggering clock edge and a clock edge occurring 320 ns later according to the setup in Fig. 2(e) in [31]. The delay was chosen four times larger than the delay at which the “jitter knee” occurs in Fig. 2(f) in [31] ($\tau_L = 1/2\pi f_L = 80$ ns) to get reliable data.

All signals on the chip are periodic with the reference frequency, so when using the frequency divider output as a triggering signal, most of the jitter due to power supply and board noise will cancel in the measurement. Such a setup gave an rms jitter of 2.5 ps at 1200 MHz, as shown in Fig. 15(b). The jitter with respect to an ideal reference would in this case be $2.5/\sqrt{2} = 1.8$ ps [31]. This proves that device noise in a standard ring oscillator is tolerable for communication standards with very tight jitter tolerances such as SONET OC-48 (2.5 Gb/s), which has a jitter specification of 4 ps rms at a 2-MHz PLL bandwidth. The VCO power consumption was 5 mW at 1200 MHz in simulation of extracted layout.

The figure of merit $\kappa$ defined in [31] is estimated from

$$\kappa = \sigma_x \cdot \sqrt{4\pi} \cdot f_L = t_{\text{min}} \cdot \sqrt{2\pi} \cdot f_L$$

(5)

where $f_L$ is the PLL bandwidth, $t_{\text{min}}$ is the measured long-term self-referenced tracking jitter, and $\sigma_x$ is the tracking jitter with respect to an ideal reference clock. Table I lists measured $\sigma_x$ and derived $\kappa$ as function of operating frequency. The jitter reported here is lower than that in [32] due to an improved measurement setup and more accurate measurement equipment. The $\kappa$ of this oscillator is better than that reported for bipolar implementations in [31] ($\kappa \approx 40\sqrt{e} - 9\sqrt{s}$) and a CMOS VCO with a $\kappa$ of $20\sqrt{e} - 9\sqrt{s}$ (as derived from the Slide Supplement of [33]). A $\kappa = 9\sqrt{e} - 9\sqrt{s}$ for a complete PLL is similar to $\kappa = 6\sqrt{e} - 9\sqrt{s}$ reported for a stand-alone VCO in [34], suggesting that noise contributions from the other PLL components (charge pump, PFD, frequency divider) are much smaller than the VCO noise. The tracking jitter compares favorably with several other CMOS oscillators [e.g., [8], [33], and [35]–[37], $\kappa$ degrades significantly at 1600-MHz operation, indicating the speed limit of the PLL. The $t_{\text{min}}$ measurements are also used for estimating the VCO period jitter ($\sigma_{VCO}$) due to device noise, based on the relation [31]

$$\sigma_{VCO} = \kappa \cdot \sqrt{T_{VCO}}$$

(6)

where $T_{VCO}$ is the VCO period. The derived period jitter agrees to within 10% of the phase noise estimation technique in [38].

The PLL tracking jitter is plotted as a function of frequency for various power-supply voltages in Fig. 16. These measurements were taken with $N = 8$ and a fixed PLL bandwidth. Since the loop filter resistance changes with $Vdd$, the chargepump reference current $I_{\text{ref}}$ in Fig. 7 was adjusted until a 3-dB PLL bandwidth of 2 MHz was measured. A bandwidth of 2
TABLE I
PLL JITTER FOR VDD = 2.5 V MEASURED WITH A PLL BANDWIDTH OF 2 MHz

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<td>4.5/53</td>
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<td>9.9</td>
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</tbody>
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*Same as Σv in [31]. **Figure of merit defined in [31]. ***Period jitter.

**Fig. 16. Tracking jitter as function of Vdd and frequency with a PLL bandwidth of 2 MHz. The right-hand scale represents the figure of merit K.**

MHz represents a scaling factor of approximately 5000 in (5), as indicated by the right-hand scale in Fig. 16.

The VCO frequency is set by the tail current in the differential delay stages and is practically independent of Vdd. Therefore, the power consumption at a fixed VCO frequency drops linearly with Vdd. The graph in Fig. 16 shows that the jitter does not change with Vdd, suggesting that power reduction (by lowering Vdd) can be achieved without jitter penalty. This seems to contradict the common belief that jitter should increase with lower power consumption. However, the critical parameter for low jitter is not power consumption but current consumption, as has previously been theoretically derived for LC oscillators [39], [40]. As shown by these measurements, low-jitter design with a fixed power budget should be based on a minimum Vdd and as large a current as can be tolerated. The measured power consumption at 250 MHz and 2.5 V is 18 mW and is dominated by buffers and the current-mode interpolator. Simulations of extracted layout indicate that the VCO consumes 0.7 mW at 250 MHz and 5 mW at 1200 MHz. The PLL characteristics are summarized in Table II.

X. CONCLUSION

Clock recovery circuits in CMOS processes require special techniques for initial frequency locking. This need is due to the fact that CMOS process variations dictate a larger frequency tuning range than can be covered by existing frequency detectors for NRZ data. An attractive technique for initial frequency locking is phase selection clock recovery, where a multioutput VCO is locked onto a reference clock and a clock recovery loop selects one of the output phases of the VCO. The large period jitter in traditional phase selection clock recovery is eliminated by the feedback phase selection technique presented here. This scheme filters the phase jumps through the PLL loop filter and also enables accurate phase interpolation with digital circuitry only, as opposed to the conventional analog-style phase interpolation.

In applications where the PLL is programmable, important loop characteristics such as bandwidth and damping factor change with the frequency multiplication mode. By making the charge-pump current depend on the division ratio in the feedback divider, a fixed bandwidth and damping factor can be obtained.

Differential analog circuits have superior supply noise rejection compared to digital complementary logic styles and are therefore preferred in an environment with large powersupply noise. However, previous differential PLL implementations have used circuits requiring large headroom, thereby prohibiting low-Vdd operation. Circuit techniques for PLL components are discussed that enable low-Vdd operation in a process technology without low-threshold devices. Correct operation has been verified down to Vdd = 0.9 V, but the lower limit for differential operation is estimated to be Vdd = Vtn + |Vq|/2 + VDSat ≈ 1.1 V in a process with measured |Vq| = 0.85 V and Vtn = 0.53 V.

Measurements show that jitter is independent of Vdd, contradicting the common belief that jitter is strongly correlated to power consumption. At a fixed operating frequency, power reduction is achieved without any penalty in jitter performance by lowering Vdd.

The tracking jitter at 500–1500 MHz was measured to be 2–5 ps rms dominated by device noise. This indicates that a standard ring oscillator can fulfill the jitter specification for a SONET OC-48 receiver.

This paper demonstrates that a clock recovery circuit with programmable bit rates can be realized with a large frequency tuning range. Robust operation and low jitter are achieved over a large range of power-supply voltages, making it ideal for low-power applications and suitable as a reusable macrocell.
REFERENCES


