Digital to Analog Converter

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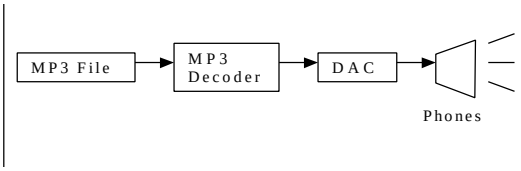
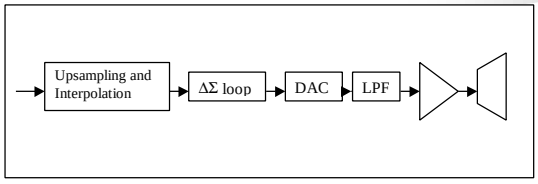
The DAC in the MP3 System



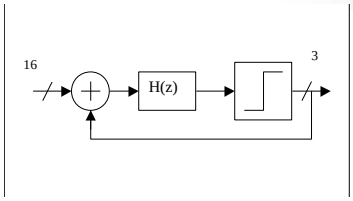
Overall DAC requirements

- Converts 16-bit samples to an analog waveform
- Accept samples at 32, 44.1 and 48kHz
- Drive a set of head-phones
- Signal to noise ratio at the output of 96dB, ideally
- Generate interrupts to request samples

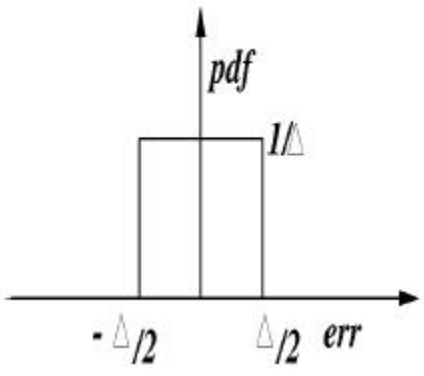
Parts of the DAC



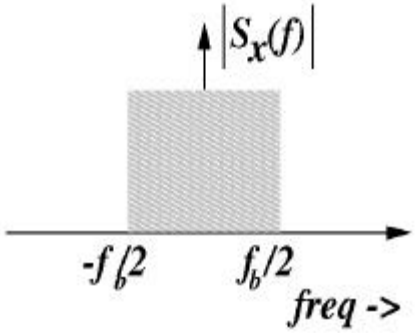
The DS Loop



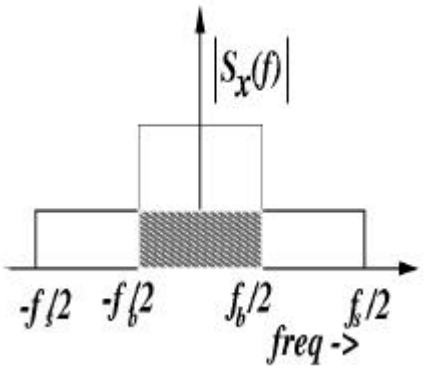
Sigma-Delta Basics



- Any ADC or DAC which has a stepsize of) can be assumed to have the quantization error pdf as shown in the adjoining figure.
- This gives the power of the error to be)^2/12.

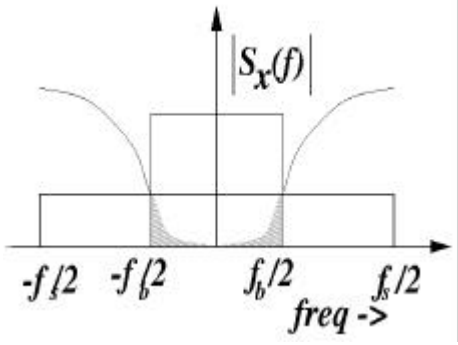


This noise is distributed in the bandwidth of the sampled signal. If the converter is at Nyquist frequency f_b then all this noise power is in the signal band.

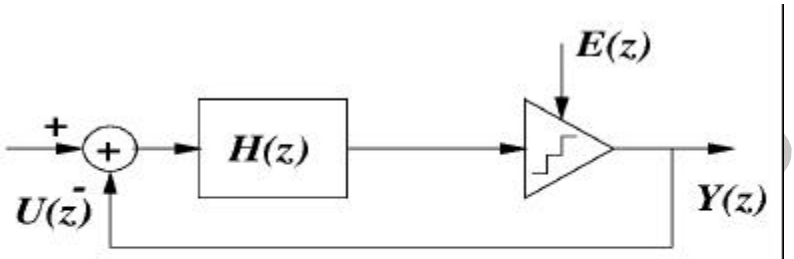


Instead if we process the signal at a frequency f_s which is larger than f_b then the same noise power would get distributed over the entire sampling bandwidth. The noise power in the signal band would however come down. This brings the noise power down by 3dB/octave of OSR (Over Sampling Ratio = f_s/f_b).

Can we do better?



We could apply a high pass filter to the noise. But, in doing so we should make sure that we don't effect the signal (at least in the expected signal bandwidth)

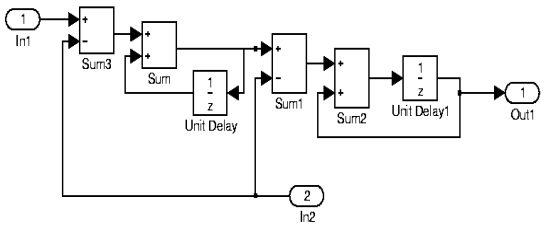


$$Y(z)/U(z) = STF = H(z)/(1-H(z))$$
$$Y(z)/E(z) = NTF = 1/(1-H(z))$$

One way to do this is with the system shown in the figure above. In order the get a high pass characteristic for the quantization signal E(z) we need the transfer function H(z) to be a low pass.

Depending on the filter order we could get much better gain than just oversampling.
1st order - 9 dB/octave
2nd order - 15 dB/octave
3rd order - 21dB/octave
assuming ideal transfer functions of $(1-z^{-1})$, $(1-z^{-1})^2$, $(1-z^{-1})^3$.
16 bit DAC requires - 96dB and if we use a 1 bit DAC and shape the noise of this DAC with a second order filter we would need an OSR of 256.
If we used a 3-bit DAC instead the same specifications would require an OSR of 64.

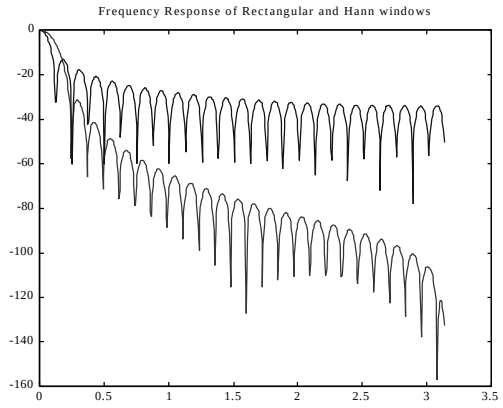
Our H(z)



Windowing and spectral estimation

- The output of the Quantizer is a discrete-time signal
- We want to determine the signal to in-band noise ratio
- By taking a finite number of points, we are "windowing" the data
- The fft of the finite set of points is a sampled version of the "real" spectrum convolved with window's frequency response

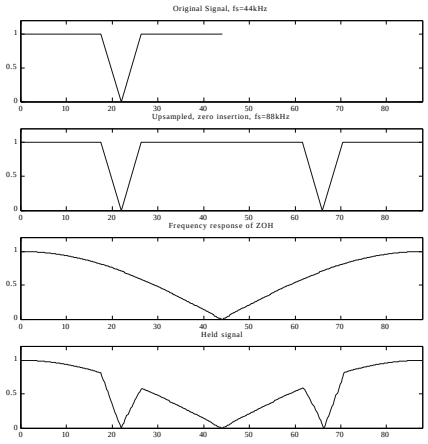
Some Windows



Interpolation

- Internals of the DAC run at a high multiple (64 for example) of the rate at which samples arrive
- Holding each input and successively sampling it generates to much out of band noise
- This will use power and may damage ears

Interpolation in the frequency domain



Interpolation

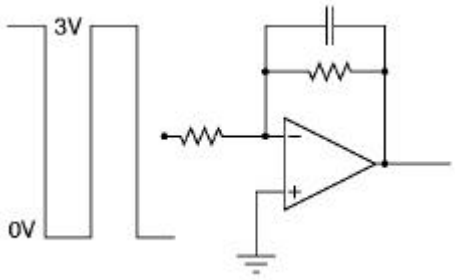
- Finite Impulse Response filters are needed to preserve the signal's phase response
- Order of an FIR is proportional to the sampling frequency divided by the transition band
- Upsampling is done in stages - The first filter will be of about order 70.
- Half Band filters have alternate coefficients equal to zero

Interpolation - Implementation

- Coefficients for HBF can be generated that are off the form $b_k=2^{-l}+2^{-m}+2^{-n}$
- This effectively eliminated multiplication

Switched Capacitor Filter

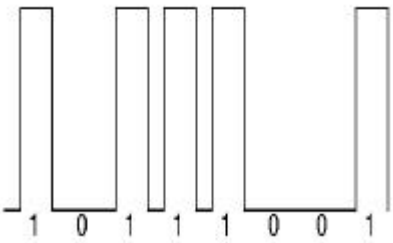
Do we REEAALLLY need it?



Yes! One bit input switching rail to rail:

- Slew of the opamp is a problem.
- If we put a cap to low pass filter then the bandwidth of the amp is very large in order to avoid inter symbol interference.
- The input rise and fall slew are required to match well.
- Any jitter in the clock pulse results in a distortion.

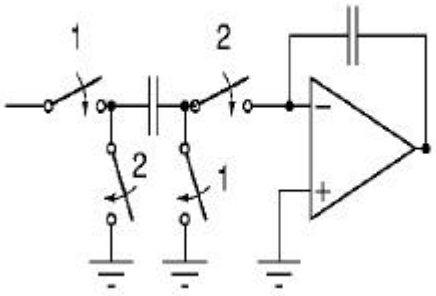
Back to zero scheme



We could use a back to zero input so that even if the output has two ones it still needs to see transitions.

But this makes the clock jitter worse as we have two transitions instead of one.

The switched capacitor advantage.



It always samples a reference voltage and if the settling is over designed the jitter would not effect the input sampling. The rise and fall rate of the selection would also not influence the amount of charge integrated.

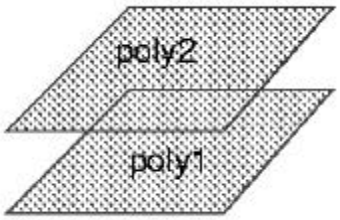
Solves all problems??

Yes and No.

A switched capacitor filter designed to have a low pass characteristic of 25kHz at the 13MHz (256*25kHz) with the bilinear transform is required to have a min/max capacitor ratio of ~ 10^4. For a smaller cap of 1pF this value is NaN.

How do we make capacitors?

Processes kind to analog designers provide a high density poly-poly caps to make capacitors.

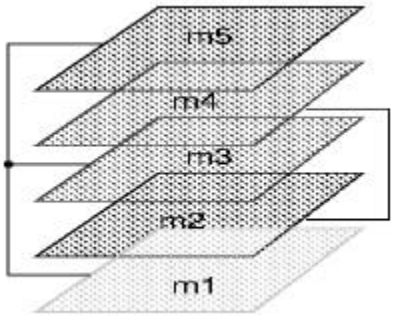


Naturally, this being a digital process does not provide the second poly.

The other possibility of making capacitors is to make metal-metal capacitors instead.

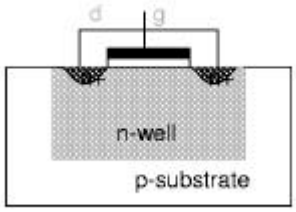
This being a *good* digital process the metal metal capacitance is low and is approximately 35aF ($a=10^{-18}$)

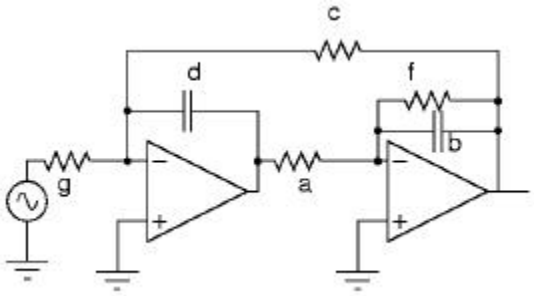
To make the smaller capacitor of 1pF we require an area of 169um*169um :-(. We could use all layers and get an improvement of 4x. (84um*84um)



Using MOS capacitors

The MOS capacitors are high density 6fF/um2~200 times metal metal caps. 1pF = 13um*13um which is easy. Problem?? Linearity of the capacitors. The linearity depends on the voltage range, but typically < 50dB for the swings we need.



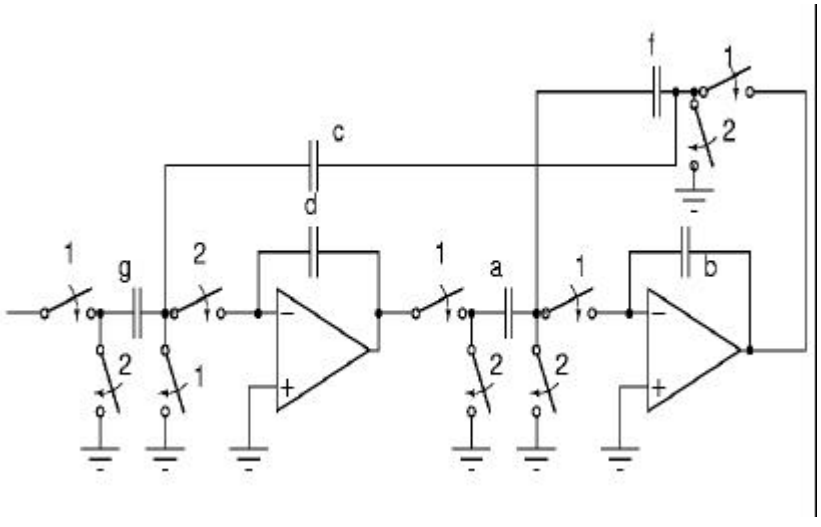


The bi-linear transform is pretty bad because it tries to implement the zeros at infinity with zeros at fs/2. Instead a use of a more reasonable LDI transform on the biquad leads to cap ratios of around a 100 between the integrating caps and the feedback caps.

What fixes the actual capacitors?

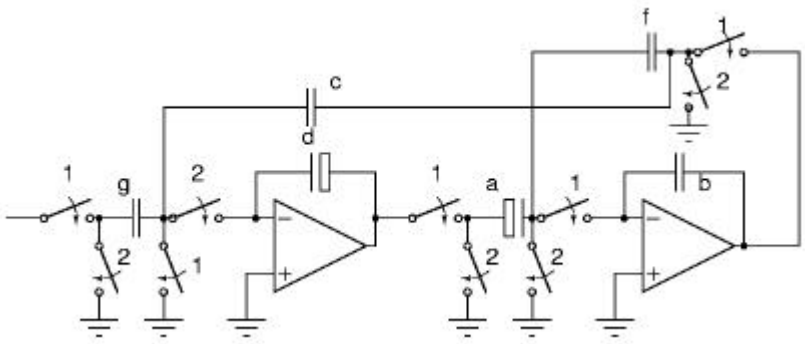
The transforms yield only capacitor ratios and the actual value of minimum capacitor is variable.
This value is fixed by the noise specification on the filter. If we are limited by just the kT/C noise this value is around 1pF for an oversampling ratio of 256.

The capacitor values required go down by the OSR because even though the noise is not shaped the inband noise is reduced by the basic oversampling phenomenon.



Best of both worlds.

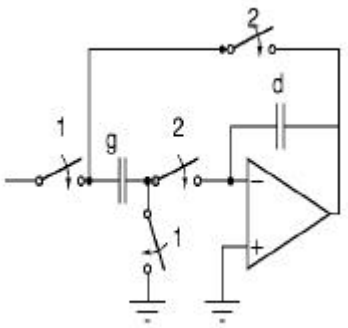
Use MOS caps for charge transfer and the linear capacitors for input and output!



We could also reduce the capacitor sizes by pushing the bandwidth that was designed for to 100kHz instead of 25kHz. We reduce the constraint that we put on the filter for reducing the out of band noise but get the following advantages.

- Phase response is better in the signal band.
- Cap ratios are more manageable ~ 20.
- The second capacitor influence on the noise is smaller so it can be made smaller and so can the second feedback capacitor with is required to be linear.

Final First order stage.



It is not possible to feed the output of the switched capacitor
stage directly to the output because although only the final
settled value matters for the switched capacitor filter the slew
does matter for the analog stage.
(The distortion is important because there is a large out of band
noise and if we mix it then it would come back to the signal band)

Is that it?

Pretty much

- Second order filter followed by the first order.
- Working with MOS capacitors makes life interesting as need to make sure that they do not mess up the dynamic range of the output and are well taken care of.
- The opamp design is kind of trivial as the noise specs are not harsh and the bandwidth is low.
- There is no estimate of the substrate coupling which the switched capacitors would be sensitive to.
- Layout of switched capacitor filters critical to the design is quite interesting and time consuming. (like MP II) .

MISMATCH-SHAPING DAC

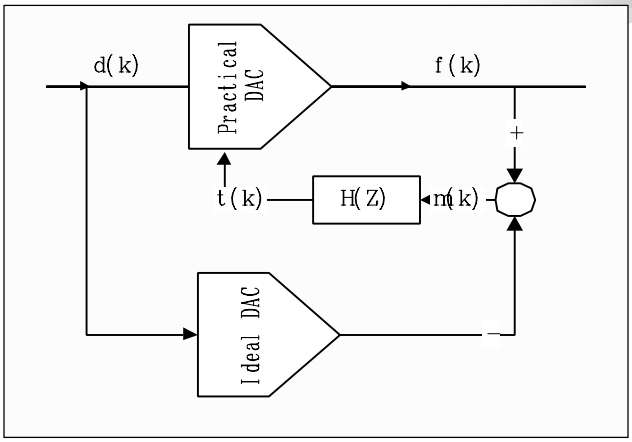
Solution for Multi-bit Delta-Sigma DAC Nonlinear

Single-bit Vs. Multi-bit in Delta-Sigma DAC

- Inherent Linear
- Bandwidth Limitation fb = fs / 2OSR
- Slew Distortion in Opamp
- Restricted Bandwith in High-resolution Application

- Nonlinear Error
- Lower OSR Needed
- Less Significant Slew in Analog End
- Solution for Nonlinear Needed

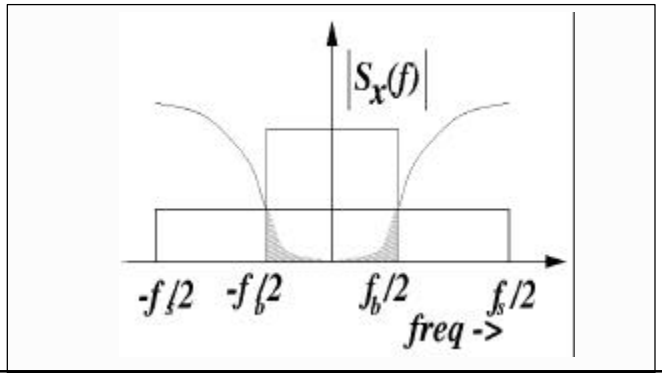
Conceptual Mismatching Shaping DAC



$$t(k) = \sum_{i=1}^{k} m(i)$$

$m(z) = (1- z^{-1})\, t(z)$

If t(k) is bounded white noise, then m(k) in the signal band can be shaped very low:



What should be done is:

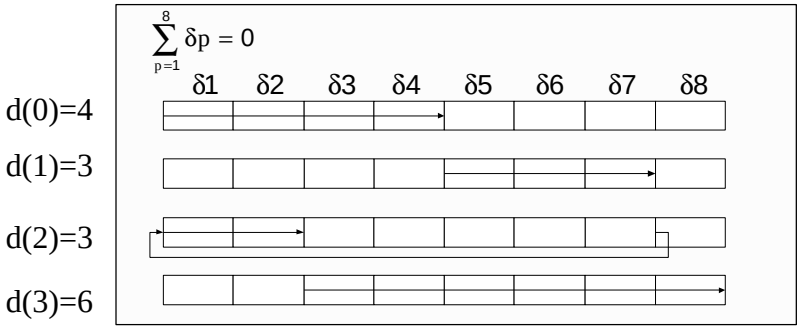
- Make t(k) bounded

  Unite-Element-Rotation-Shaping
  Unite-Element-tree-Structure Shaping
- Make t(k) aperiodic, approaching White Noise

  Dithered Encoder

Element-Rotation Scheme

By rotating the 8 bit unit elements, each of them is almost used at the same frequency, the accumulation error never exceeds one round.



Dithered UE-MS Encoder

By radomly switching the ERS path, The correlationship between d(k) and t(k) (accumulation error) is eleminated, no tone in t(k).