Columbia Univerity
Department of Electrical Engineering
Spring, 1999

Course: EE E4340. Computer Hardware Design.

Instructor: Ken Shepard

E-mail: shepard@ee.columbia.edu

Office: 1019 CEPSR

Office hours: MW 2:00 - 4:00 PM

Class webpage: `http://www.vlsi.columbia.edu/ee4340`

Texts:

- Hayes, *Computer Architecture and Organization*, McGraw-Hill.
- Bhaskar, *VHDL Primer*, Prentice-Hall.

References:

- Hennessy and Patterson, *Computer Organization: A Quantitative Approach*, Morgan-Kaufmann.
- Prosser and Winkel, *The Art of Digital Design*, Prentice-Hall.
- Walkerly, *Digital Design: Principles and Practices*, Prentice-Hall.
- Dally and Poulton, *Digital systems engineering*, Cambridge University Press.
- Salcic and Smailagic, *Digital systems design and prototyping using field-programmable logic*, Kluwer.

- Ercegovac and Lang, *Digital systems and hardware/firmware algorithms*, Wiley.
- Ashenden, *The Designer's Guide to VHDL*, Morgan Kaufmann.

Grading:

- HW/Lab Sets: 30%
- Midterm Quiz: 20%
- Final project report and presentation: 30 %
- Final Exam: 20%

Lectures

- Week 1. Course introduction. What is a computer? Instruction set architectures.
- Week 2. Assembly language and instruction sets (con't). PDP/8 architecture.
- Week 3. Design methodology and processes. Cost issues. ASM charting and state machine design.
- Week 4. Fundamentals of VHDL.
- Week 5. Datapath design and the requirements of the instruction set. Datapath elements. PDP/8 datapath.
- Week 6. Memory. Buses and I/O system design. Asynchronous communication discipline. UARTs.
- Week 7. Control logic design. Hardwired control, microcode, millicode.
- Week 8. Control logic for the PDP/8. Testing and validation of hardware.

- Week 9. Logic families and programmable logic. FPGAs.
- Week 10. Power, timing, noise issues in digital design.
- Week 11. Performance. CPI and cycle time. Pipelining. (Extensive lab work)
- Week 12. Multiprocessors. (Extensive lab work)
- Week 13-14. Final presentations.

Homeworks/Laboratories

- Week 1-2. PDP-8 assembly language programming.
- Week 2-3. VHDL and state machine design.
- Week 4-5. Implementation and verification of the PDP-8 datapath.
- Week 6-8. Implementation and verification of the PDP-8 controls.
- Week 9-11. Program FPGAs and debug front panel.
- Week 12. Debug serial port.
- Week 13. Load FOCAL and test.
- Week 14. Final presentations.