Columbia University
Department of Electrical Engineering
EE E4340. Homework/Laboratory #4.
PDP-8 Fetch controls.
Due: March 9, 1999

In subsequent homeworks/laboratories, you will be building up the hard-wired control logic of the PDP-8. For this and all subsequent homework/laboratory assignments, you should pair off and work as groups of two. In this homework, you will write VHDL for the fetch controls of the PDP-8 that we went over in class.

First a correction to the datapath specification of the previous homework. For `mem_interface`, if `jms0` is high, then the mem drivers are tristated and `data_out` is driven to `"100000000000"` which is a $JMS0$ instruction.

In your VHDL, please assume that there is a debounced switch input `cont`, which you must synchronize and pulse. You may "deadend" your controls for now by making the `E0` state the `IDLE` state, or you could enable continuous operation by making the `E0` state the `F1` state. Create a single symbol for your control logic and wire it up to the dataflow you created in Homework #3. In addition, wire up three 2168 SRAM chips to the memory bus in your schematic. Each SRAM will provide four bits of the twelve bit word. You will find a component for this called `sram_2168` in the library `pdp8` in `/user/ee4332/pdp8`.

Create a testbench for your design. You might want to do your testing by loading up memory with an instruction stream and verifying that each instruction in the stream is correctly fetched.