Columbia University
Department of Electrical Engineering
EE E4340. Homework/Laboratory #2.
ASM charting and VHDL modelling.
Due: February 16, 1999

Before you begin this homework/laboratory assignment, you will want to go through the Composer/Leapfrog tutorial to become familiar with the design environment and the tools which will be required to complete this assignment. The tutorials will probably take 6-8 hours to complete so please plan accordingly.

In this assignment, your boss has asked you to design the logic for a kitchen timer which will be implemented as an ASIC. This might make sense from a business perspective if the timer has very high volumes and can be manufactured sufficiently cheaply. Otherwise, a general-purpose microcontroller with some software might be more appropriate for this application.

1 Timer specification

The timer supplies two independent countdown timers, each of which can get set by incrementing minutes or seconds. The timer begins on command and operates a buzzer, which turns off when any button is pressed. Both timers work off of the same display. The display has four digits (two for minutes and two for seconds). Each digit is displayed with seven segments. The inputs of your chip are:

- `timer1`. Comes from a button and selects Timer 1 for display, programming, or countdown.
- `timer2`. Comes from a button and selects Timer 2 for display, programming, or countdown.
- `minutes`. Comes from a button and increments the selected timer in minute increments.
- `seconds`. Comes from a button and increments the selected timer in second increments.

- `clear`. Comes from a button and clears the selected timer.
- `go`. Comes from a button and starts counting down the selected timer.
- `clock`. A 1kHz global clock.

The outputs are:

- `segments0<0:6>` Driver signals for the seven segments of the first digit of the display.
- `segments1<0:6>` Driver signals for the seven segments of the second digit of the display.
- `segments2<0:6>` Driver signals for the seven segments of the third digit of the display.
- `segments3<0:6>` Driver signals for the seven segments of the fourth digit of the display.
- `buzz`. Driver signal for the buzzer.

You may assume that all switches have been debounced.

2 Micro-architecture

Design a micro-architecture for your design. One possible component hierarchy for the design shown in Figure 1. Create schematics in Cadence to capture your design. You will only need to enter "text" VHDL for the leaf-cell components (`controller`, `buzz`, `timerOne`, `timerTwo`, and `display` for this micro-architecture).

3 Verification

You are to run extensive simulations on your design with a VHDL testbench to verify that it functions correctly.

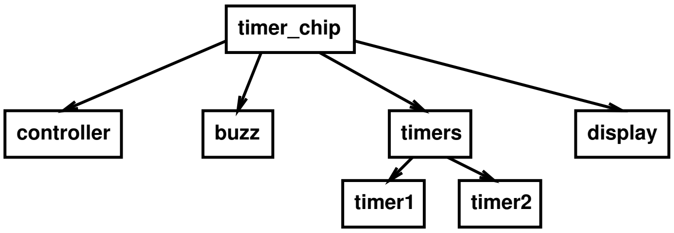

Figure 1: Possible component hierarchy for the kitchen timer

4 What to turn in

Please turn in your complete VHDL, including your testbench (this can be easily exported from the Cadence Composer interface). Include a brief description of your micro-architecture. Please also hand-in the ASM charts for your controller design. You should also turn in a description of the functional testing you did for your design, and any waveform plots or other results to substantiate this testing.